

200G QSFP28-DD to QSFP28-DD LPO AOC

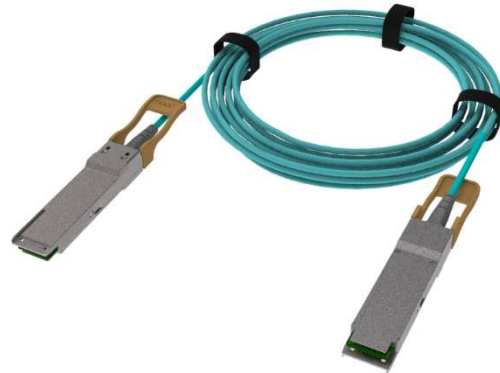
PN: V2C-D1DyyyC-QA

Product Overview

The V2C-D1DyyyC-QA is a 200G QSFP28-DD to QSFP28-DD Linear Pluggable Optics (LPO) Active Optical Cable (AOC). It supports 25.78Gb/s data rates per channel, utilizing an integrated 850nm VCSEL array and PD array without onboard DSP or CDR. This hot-pluggable AOC is designed in a QSFP-DD form factor, compliant with QSFP-DD HW Rev6.2 and CMIS 4.0 specifications. It features a maximum power consumption of 3.5W per end, operates on a single 3.3V power supply, and is specified for a case operating temperature range of 0°C to 70°C.

Features

- 25.78Gb/s data rate per channel
- Integrated 850nm VCSEL array and PD array w/o DSP or CDR
- Hot-pluggable QSFP-DD form factor
- Compliant to QSFP-DD HW Rev6.2
- Compliant with CMIS 4.0
- Maximum power consumption 3.5W(each end)
- Single 3.3V power supply
- Case operating temperature 0°C to 70°C
- Class 1 laser
- RoHS complaint



Ordering Information

Part Number	Description
V2C-D1DyyyC-QA	200G QSFP28-DD to QSFP28-DD LPO AOC



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T _s	-40	85	°C	
Power Supply Voltage	V _{cc}	-0.3	3.6	V	
Relative Humidity (non-condensing)	RH	5	85	%	

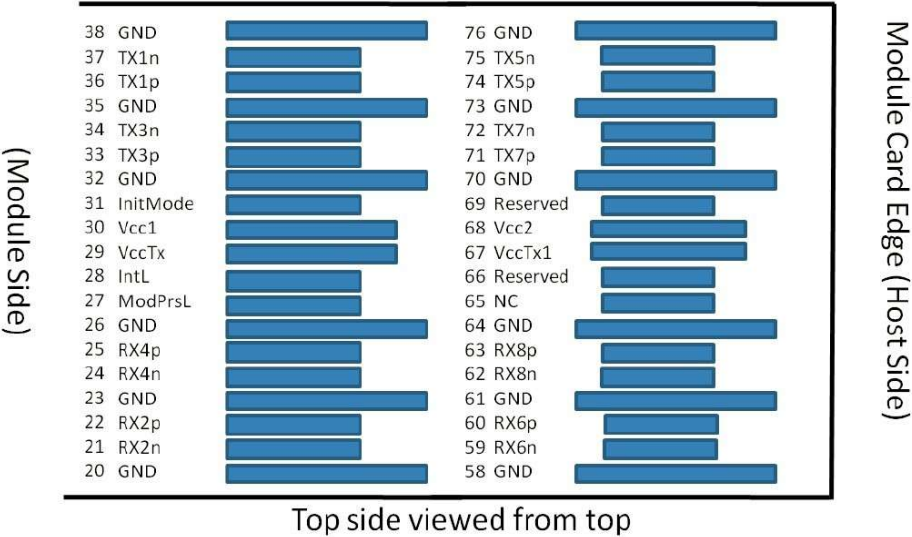
Recommended Operating Conditions

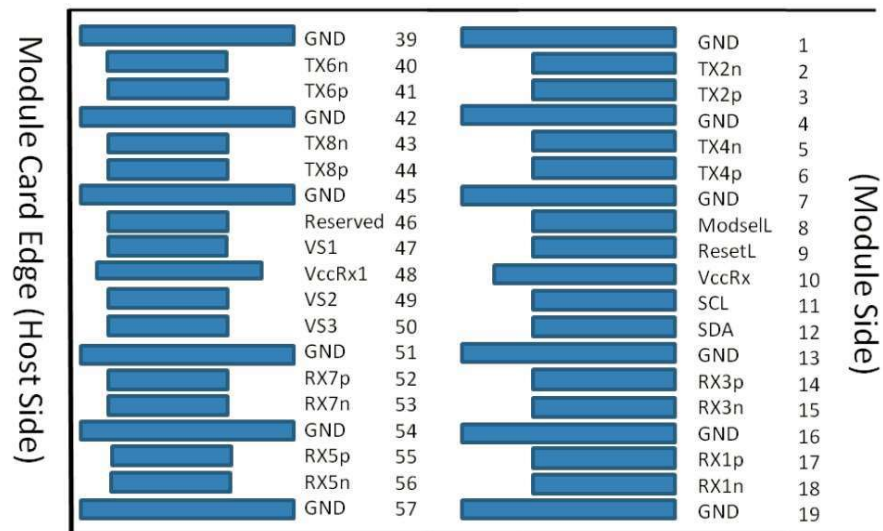
Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOPR	0	-	70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Lane Baud Rate	BRLANE		25.78125		Gbps
Maximum Power Consumption (each end)	Pmax			3.5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Z _{in}		100		ohm
Differential Output impedance	Z _{out}		100		ohm
Differential input voltage amplitude	ΔV _{in}	200	-	900	mVp-p
Differential output voltage amplitude	ΔV _{out}	400	-	800	mVp-p
Pre-FEC Bit Error Ratio				5E-5	

Electrical Connector Layout





Bottom side viewed from bottom

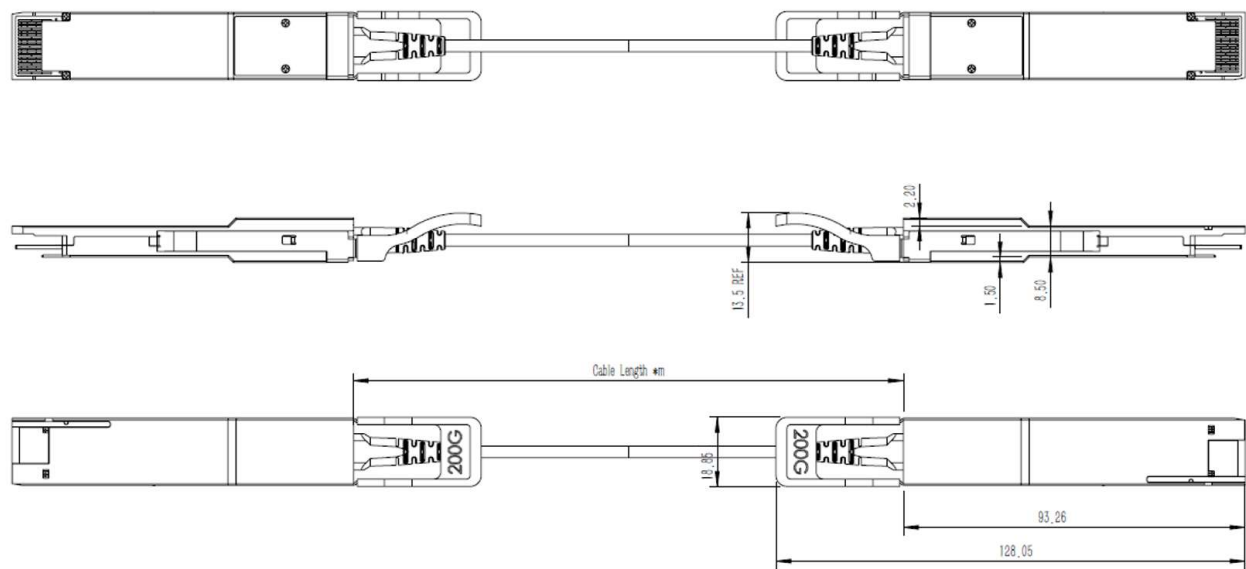
Electrical Pin Definition

Pin	Logic	Symbol	Description	Pin#	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVC MOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVC MOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output

18	CML-O	RxIn	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground



Mechanical Dimensions



Revision History

Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

For more information

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