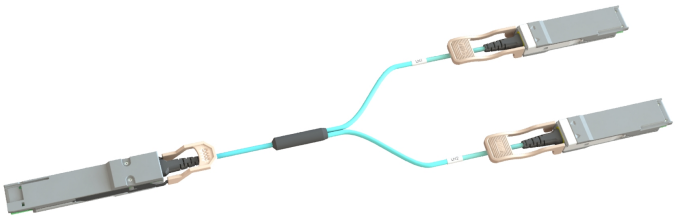
200G QSFP-DD to 2x 100G QSFP28 Duplex Breakout AOC
PN: V2C-D2QyyyC-AA

Product Overview

Vitex V2C-D2QyyyC-AA is a parallel 200G SR8 based 8-lane QSFP28-DD to 2x100G SR4. The use and replacement of breakout AOC is simple and straightforward as it adopts the standard QSFP28-DD form factor and complies to MSA specifications. The product provides an onboard MCU that allows access to full monitoring and configuration data via the 2-wire Management Interface.

Features

- 200G-SR8 QSFP28-DD to 2x 100G-SR4 QSFP28 breakout
- Full duplex 25.78 Gb/s per channel
- 10 Gb/s operation with CDR bypass
- Up to 100m with OM3/OM4 fiber
- Single 3.3V power supply
- Power consumption 4W QSFP28-DD side
  - 2.5W QSFP28 side
- Digital Diagnostic Monitoring (DDM) support
- Commercial operating temperature: 0°C to +70°C
- LSZH cable
- Hot Pluggable QSFP-DD form factor, QSFP-DD MSA CMIS 4.0 compliant
- Compliant with RoHS2.0



Applications

- IEEE 802.3bs 200G-SR8 and IEEE 802.3bm 100G-SR4
- Data centers (Servers, Switches, Storages)
- Cell site router and server connectivity
- Proprietary HPC interconnects

Ordering Information

Part Number	Description
V2C-D2QyyyC-AA	200G-SR8 QSFP-DD to 2x 100G-SR4 QSFP28 Breakout AOC, yyym, DDM, C-temp (yyy is cable length in meters)
V2C-D2Q003C-AA	200G-SR8 QSFP-DD to 2x 100G-SR4 QSFP28 Breakout AOC 3m, DDM, C-temp

General Specifications

Parameter		Symbol	Min	Typical	Max	Unit
Storage Temperature		T_S	-40		85	°C
Relative Humidity		R_H	5		85	%
Supply Voltage		V_S	0		4	V
Operating Case Temperature		T_C	0		70	°C
Operating Supply Voltage		V_{CC}	3.13	3.3	3.47	V
Power Consumption	QSFP28-DD	P			4	W
	QSFP28				2.5	
Data Rate		DR	25.78125±100ppm			Gb/s
Bit Error Rate [1]		BER			5E-5	

1. Pre-FEC Bit Error Ratio with a PRBS 2^{31-1} test pattern

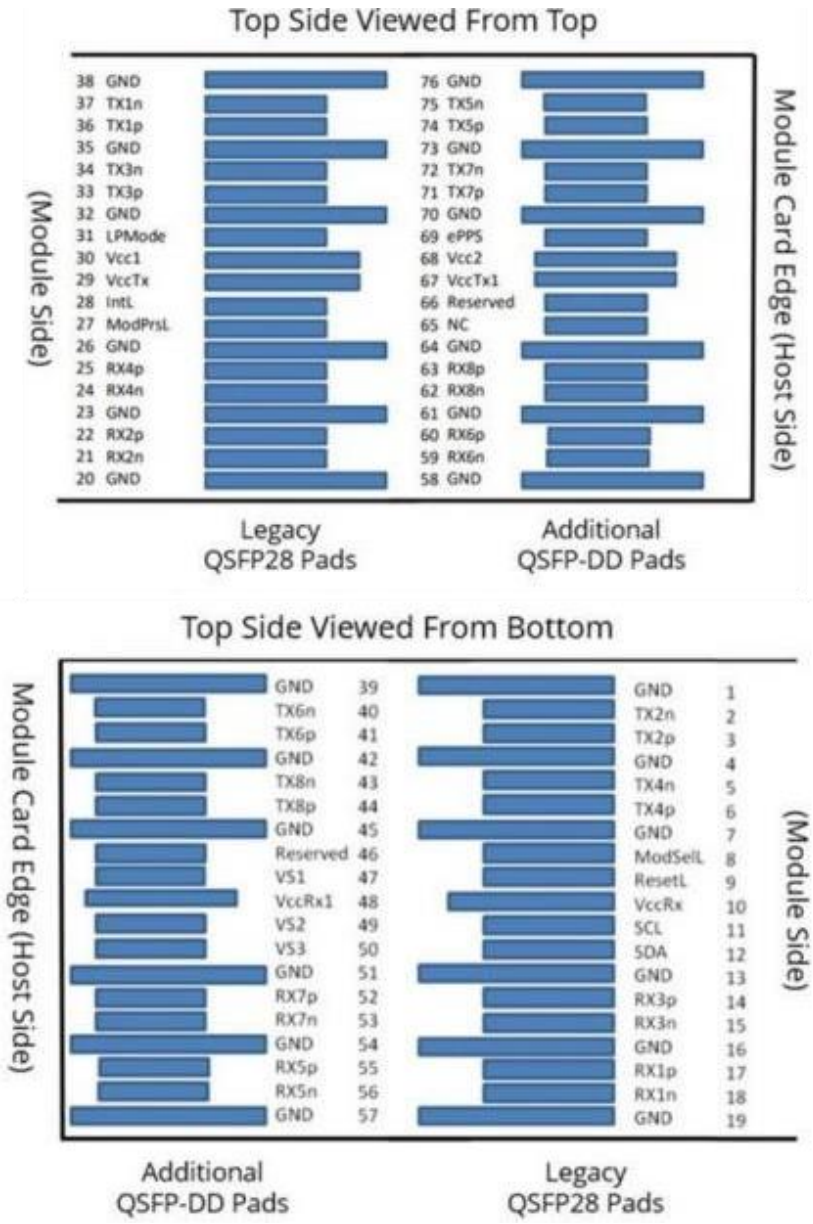
Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit
Input Differential Impedance	R_{IN}	90	100	110	Ω
Differential Data Input Voltage	V_{INP-P}	200		900	mV
Modulation Format	NRZ				
Transmit Disable Voltage	V_{DIS}	2		V_{CCHOST}	V
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V
Transmit Fault Assert	V_{FA}	2		V_{CCHOST}	V
Transmit Fault De-Assert	V_{FDA}	V_{EE}		V_{EE}+0.8	V

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit
Output Differential Impedance	R_{OUT}	90	100	110	Ω
Differential Data Input Voltage	V_{OUTP-P}	200		500	mV
LOS Fault	V_{LOSF}	2		V_{CCHOST}	V
LOS Normal	V_{LOSN}	V_{EE}		V_{EE}+0.8	V

Electrical Connector Layout



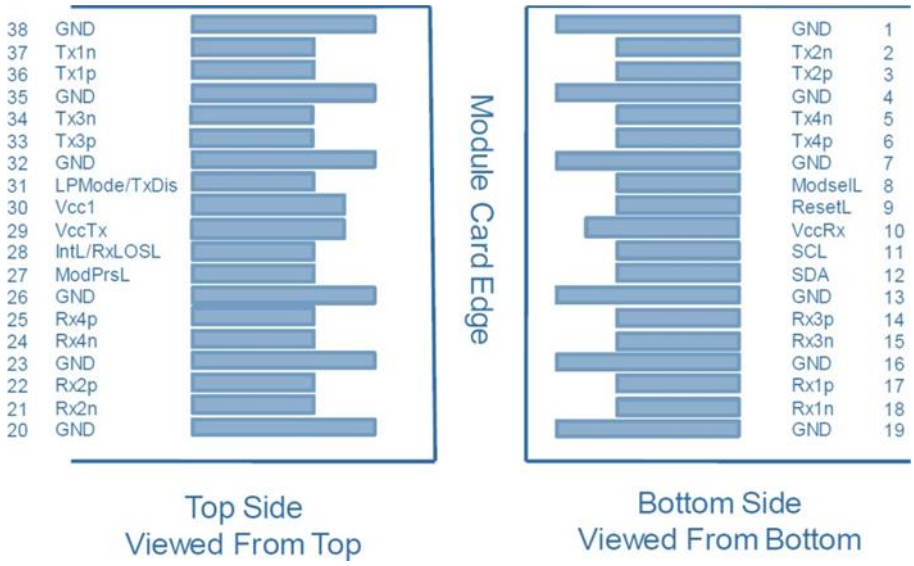
Electrical Pin Definition for QSFP-DD

PIN #	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-wire Serial Interface Clock	
12	SDA	2-wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V Power Supply Transmitter	2
30	Vcc1	3.3V Power Supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1

43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply Receiver	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V Power Supply Transmitter	2
68	Vcc2	3.3V Power Supply	2
69	ePPS	Precision Time Protocol (PTP) reference clock input	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal- common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Pin Description – QSFP28



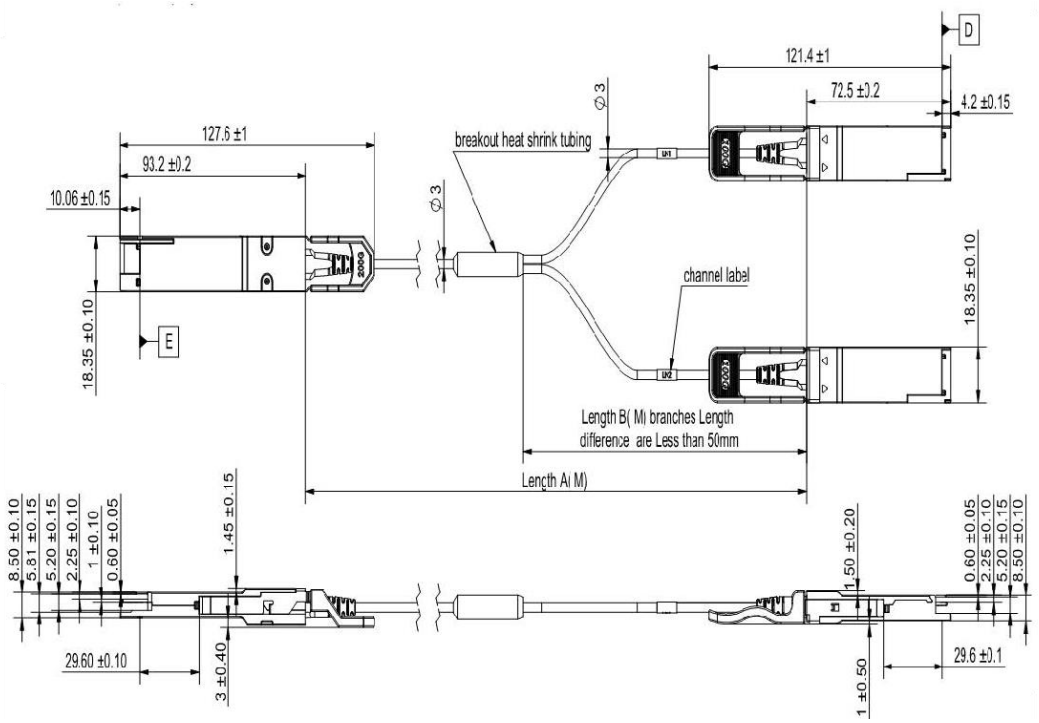
Electrical Pin Definition – QSFP28

Pin	Symbol	Description	Unit
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2-	Transmitter Inverted Data Input	
3	Tx2+	Transmitter Non-Inverted Data Input	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4-	Transmitter Inverted Data Input	
6	Tx4+	Transmitter Non-Inverted Data Input	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	2
9	ResetL	Module Reset	2
10	VccRx	3.3V Power Supply Receiver	
11	SCL	2-Wire serial Interface Clock	2
12	SDA	2-Wire serial Interface Data	2
13	GND	Transmitter Ground (Common with Receiver Ground)	1
14	Rx3+	Receiver Non-Inverted Data Output	
15	Rx3-	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1+	Receiver Non-Inverted Data Output	
18	Rx1-	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2-	Receiver Inverted Data Output	
22	Rx2+	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1

24	Rx4-	Receiver Inverted Data Output	1
25	Rx4+	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	2
29	VccTx	3.3V Power Supply Transmitter	
30	Vcc1	3.3V Power Supply	
31	LPMode	Low Power Mode	2
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3+	Transmitter Non-Inverted Data Input	
34	Tx3-	Transmitter Inverted Data Input	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1+	Transmitter Non-Inverted Data Input	
37	Tx1-	Transmitter Inverted Data Input	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

1. The module uses common ground (GND) for all signals and supply (power). All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1, and VccTx shall be applied concurrently, and may be internally connected within the module in any combination.

Mechanical Dimensions



PN	Length (A)	Tolerance (A)	Length (B)	Tolerance (B)
V2C-D2Q010C-AA	10m	+0.4/0m	3m	+0.3/0m

Revision History

Date	Rev	Description
09/23/2022	1.0	Initial Release
04/12/2023	2.0	Updated Logo and Formatting
07/06/2023	2.1	Minor Corrections to Logo and Formatting
08/02/2023	2.2	Updated Mechanical Diagrams
08/21/2023	2.3	Corrected Specifications.

For more information

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