
400G QSFP56-DD to 4x 100G QSFP56 AOC

PN: V4C-D4QyyyC-AA

Product Overview

The V4C-D4QyyyC-AA is a 400G QSFP56-DD to 4x 100G QSFP56 Active Optical Cable (AOC) that supports data rates up to 53Gbps per channel using PAM4 modulation. It features a 400GAUI-8 electrical interface on the QSFP-DD end and a 200GAUI-4 electrical interface on each of the four QSFP56 ends. The AOC incorporates integrated 850nm VCSEL and PD arrays within its hot-pluggable QSFP-DD and QSFP56 form factors. It has a maximum power consumption of 4.5W for the QSFP-DD end and 3.5W for each QSFP56 end and operates on a single 3.3V power supply.

Features

- Up to 53Gbps data rate per channel by PAM4 modulation
- 400GAUI-8 electrical interface for QSFP-DD end
- 200GAUI-4 electrical interface for QSFP end
- Integrated 850nm VCSEL array and PD array
- Hot-pluggable QSFP-DD form factor and QSFP56 form factor
- Compliant to QSFP-DD HW Rev6.2 and QSFP MSA
- Supported CMIS 4.0 for QSFP-DD end
- Supported CMIS 4.0 or SFF 8636 for QSFP end
- Maximum power consumption 4.5W for QSFP-DD end and 3.5W for QSFP end
- Single 3.3V power supply
- Case operating temperature 0°C to 70°C
- Class 1 laser
- RoHS compliant

Ordering Information

Part Number	Description
V4C-D4QyyyC-AA	400G QSFP56-DD to 4x 100G QSFP56 AOC, yyy in meters

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Power Supply Voltage	VCC	-0.3	3.6	V	
Control Input Voltage	VI	-0.3	3.465	V	
Relative Humidity (non-condensing)	RH	15	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOPR	0	-	70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Maximum Power Consumption (QSFP-DD)	Pmax			5	W
Maximum Power Consumption (QSFP)	Pmax			3	W

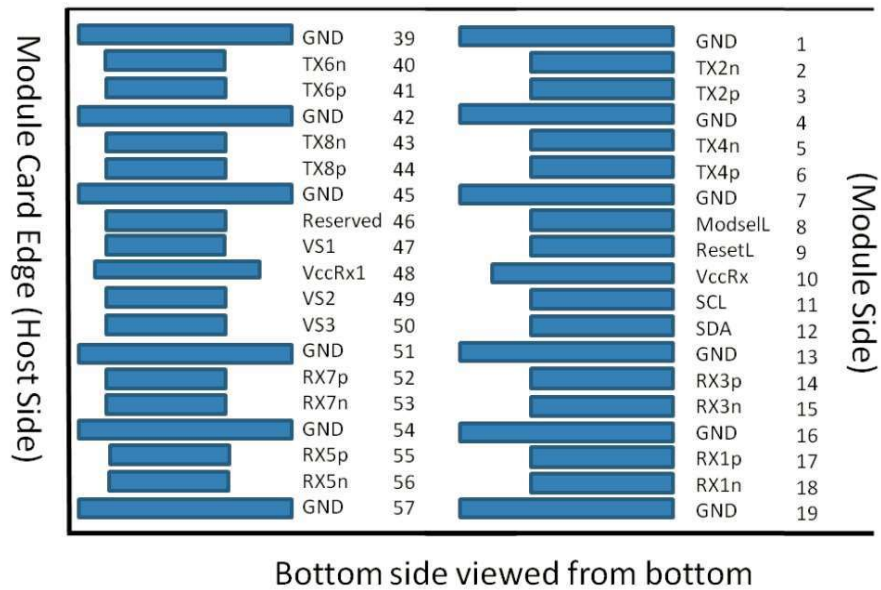
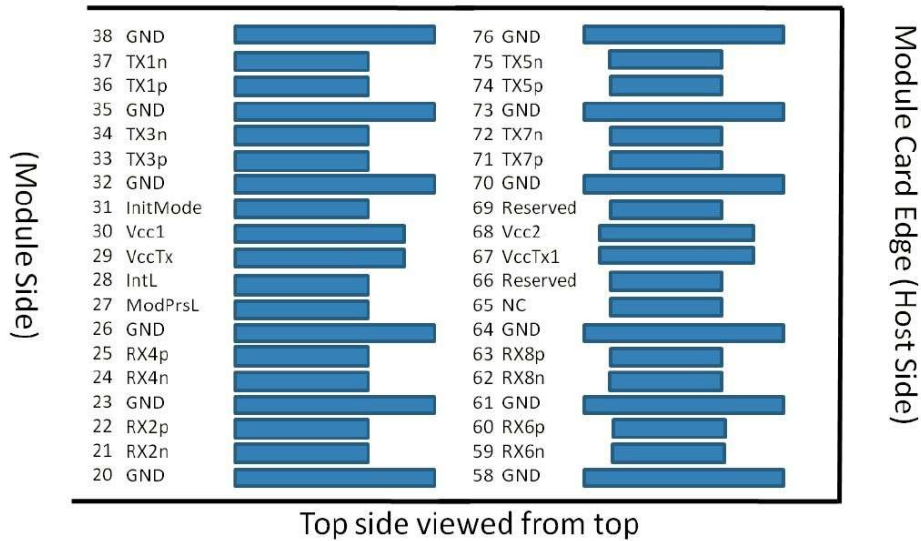
Electrical Specifications Low Speed Signal

Parameter	Symbol	Min	Typical	Max	Unit
Module output SCL and SDA	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	
Module Input SCL and SDA	V _{IL}	-0.3	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	V _{CC} +0.5	V	
LPMode/TxDis, ResetL, ModSelL and ePPS/Clock	V _{IL}	-0.3	0.8	V	
	V _{IH}	2	V _{CC} +0.3	V	
IntL/RxLOS	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	

Electrical Specifications High Speed

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling Rate per Lane	SRL	-	26.5625	-	GBd	PAM4
AC common-mode output voltage				17.5	mV	
Differential peak-to-peak output voltage				900	mV	
DC common mode voltage	-350			2850	mV	
Pre-FEC BER				1E-5		

Electrical Connector Layout QSFP-DD End

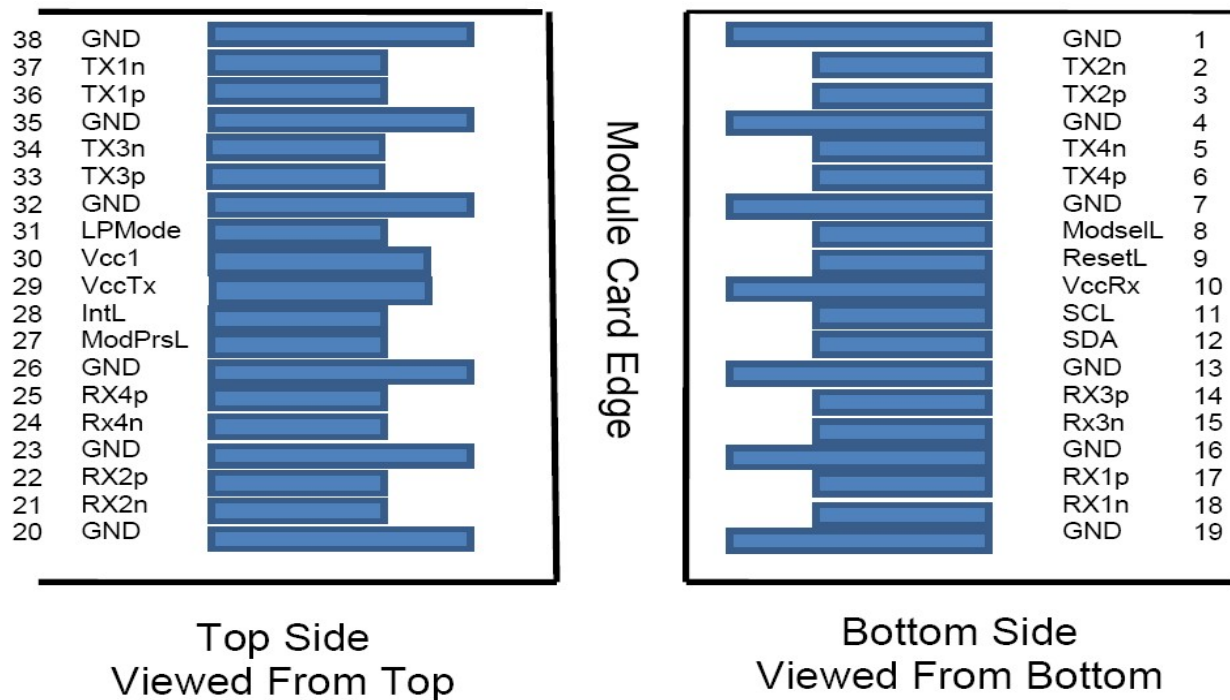


Pin #	Logic	Symbol	Description	Pin #	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground

5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVC MOS -I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVC MOS -I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		VccI	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input

34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Txlp	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Txln	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

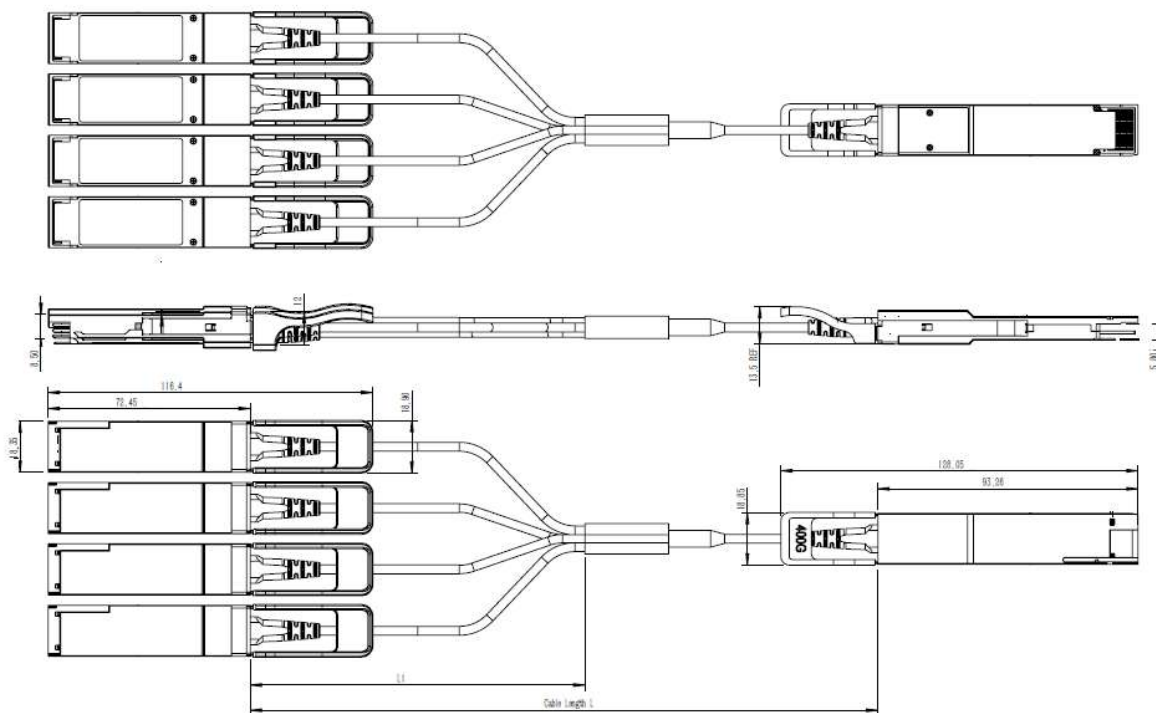
Electrical Connector Layout QSFP End



Electrical Pin Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	

12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		VccI	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	



Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

