400G OSFP to 4xQSFP56 AOC
PN: V4C-P4QyyC-ANA

Product Overview

The V4C-P4QyyC-ANA is a 400G OSFP to 4x100G QSFP56 Active Optical Cable (AOC) designed for high-density breakout applications. It supports data rates up to 53.125Gbps (PAM4) per channel, facilitating a 400G to 4x100G split. The OSFP end adheres to CMIS 4.0 specifications, while the QSFP56 end with SFF-8636. The cable operates with a single 3.3V power supply, maintaining a case operating temperature range of 0°C to 70°C. Power consumption is specified at a maximum of 10W for the OSFP end and 3W for each QSFP56 end.

Features

- 400G OSFP to 4*100G QSFP56 Breakout
- Data Rate up to 53.125Gbps (PAM4) per channel
- Maximum power consumption: 10W for OSFP end & 3W for QSFP56 end
- OSFP end compliant with CMIS 4.0
- QSFP56 ends compliant with SFF-8636
- Case operating temperature 0°C to 70°C
- Single 3.3V power supply
- Hot pluggable
- RoHS compliant

Ordering Information

Part Number	Description
V4C-P4QyyC-ANA	400G OSFP to 4xQSFP56 AOC, yyy in meters

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{CC}	-0.3	3.6	V	
Relative Humidity (non-condensing)	RH	5	85	%	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	

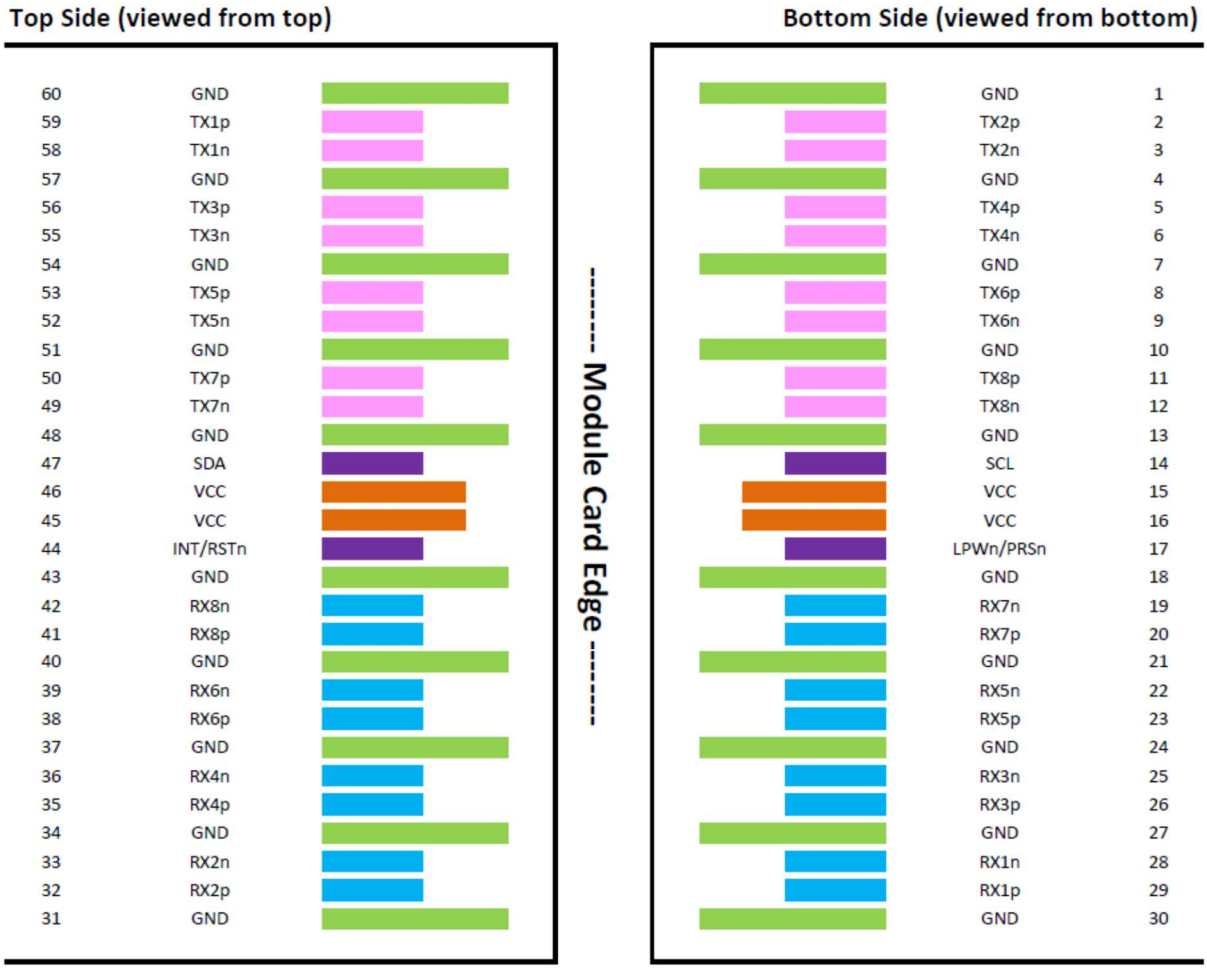
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Maximum Power Dissipation (OSFP end)	P_D			10	W	
Maximum Power Dissipation (QSFP56 end)	P_D			3	W	
Signaling Rate per Lane	SRL		26.5625		GBd	PAM4

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling Rate per Lane	SRL		26.5625		GBd	PAM4
AC common-mode output voltage				17.5	mV	
Differential peak-to-peak output voltage				900	mV	
DC common mode voltage	–350			2850	mV	
Pre-FEC BER				1E-5		

Electrical Connector Layout OSFP End

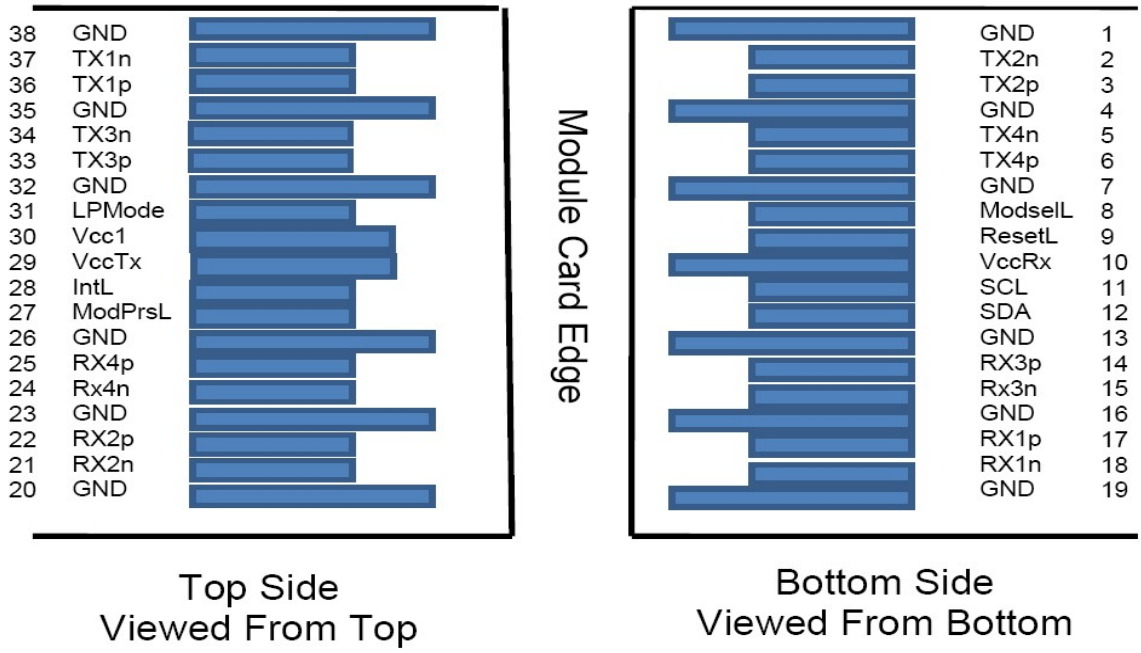


Electrical Pin Definition

Pin #	Logic	Symbol	Description	Direction	Plug Seq	Notes
1		GND	Ground		1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	Input from Host	3	
3	CML-I	TX2n	Transmitter Data Inverted	Input from Host	3	
4		GND	Ground		1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	Input from Host	3	
6	CML-I	TX4n	Transmitter Data Inverted	Input from Host	3	
7		GND	Ground		1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	Input from Host	3	
9	CML-I	TX6n	Transmitter Data Inverted	Input from Host	3	
10		GND	Ground		1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	Input from Host	3	
12	CML-I	TX8n	Transmitter Data Inverted	Input from Host	3	
13		GND	Ground		1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Bi-directional	3	
15		VCC	+3.3V Power	Power from Host	2	
16		VCC	+3.3V Power	Power from Host	2	

17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	3	
18		GND	Ground		1	
19	CML-O	RX7n	Receiver Data Inverted	Output to Host	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	Output to Host	3	
21		GND	Ground		1	
22	CML-O	RX5n	Receiver Data Inverted	Output to Host	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	Output to Host	3	
24		GND	Ground		1	
25	CML-O	RX3n	Receiver Data Inverted	Output to Host	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	Output to Host	3	
27		GND	Ground		1	
28	CML-O	RX1n	Receiver Data Inverted	Output to Host	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	Output to Host	3	
30		GND	Ground		1	
31		GND	Ground		1	
32	CML-O	RX2p	Receiver Data Non-Inverted	Output to Host	3	
33	CML-O	RX2n	Receiver Data Inverted	Output to Host	3	
34		GND	Ground		1	
35	CML-O	RX4p	Receiver Data Non-Inverted	Output to Host	3	
36	CML-O	RX4n	Receiver Data Inverted	Output to Host	3	
37		GND	Ground		1	
38	CML-O	RX6p	Receiver Data Non-Inverted	Output to Host	3	
39	CML-O	RX6n	Receiver Data Inverted	Output to Host	3	
40		GND	Ground		1	
41	CML-O	RX8p	Receiver Data Non-Inverted	Output to Host	3	
42	CML-O	RX8n	Receiver Data Inverted	Output to Host	3	
43		GND	Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	3	
45		VCC	+3.3V Power	Power from Host	2	
46		VCC	+3.3V Power	Power from Host	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	Bi-directional	3	
48		GND	Ground		1	
49	CML-I	TX7n	Transmitter Data Inverted	Input from Host	3	
50	CML-I	TX7p	Transmitter Data Non-Inverted	Input from Host	3	
51		GND	Ground		1	
52	CML-I	TX5n	Transmitter Data Inverted	Input from Host	3	
53	CML-I	TX5p	Transmitter Data Non-Inverted	Input from Host	3	
54		GND	Ground		1	
55	CML-I	TX3n	Transmitter Data Inverted	Input from Host	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	Input from Host	3	
57		GND	Ground		1	
58	CML-I	TX1n	Transmitter Data Inverted	Input from Host	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	Input from Host	3	
60		GND	Ground		1	

Electrical Connector Layout QSFP56 End

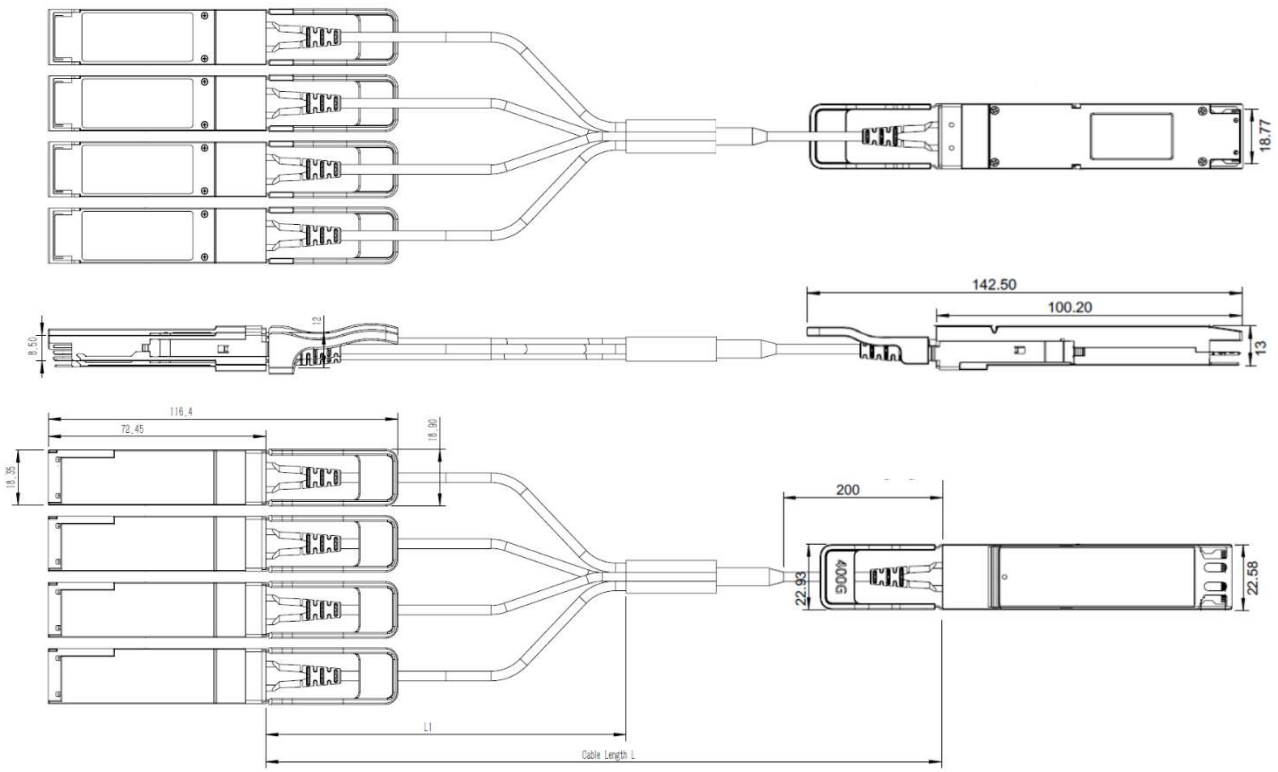


Electrical Pin Definition

Pin #	Logic	Symbol	Description	Plug Seq	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	Not used
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	Not used
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	Not used
15	CML-O	Rx3n	Receiver Inverted Data Output	3	Not used
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	

24	CML-O	Rx4n	Receiver Inverted Data Output	3	Not used
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	Not used
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	Not used
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	Not used
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

Mechanical Dimensions



Parameter	Value	Unit
Diameter	3±0.2	mm
Minimum bend radius	30	mm
Length tolerance	1m≤length<5m: +15/-0	cm
	5m≤length<15m: +30/-0	cm
	length>15.0m: +3%/-0	m
Cable color	Aqua	

Connectivity Schematic			
400G OSFP end	TX1	RX1	QSFP56 end1
	TX2	RX2	
	RX1	TX1	
	RX2	TX2	
	TX3	RX1	QSFP56 end2
	TX4	RX2	
	RX3	TX1	
	RX4	TX2	
	TX5	RX1	QSFP56 end3
	TX6	RX2	
	RX5	TX1	
	RX6	TX2	
	TX7	RX1	QSFP56 end4
	TX8	RX2	
	RX7	TX1	
	RX8	TX2	

Revision History

Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

For more information

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