800G QSFP-DD800 to QSFP-DD800 AOC
PN: V8C-D1DyyyC-AA

Product Overview

The V8C-D1DyyyC-AA is an 800G QSFP-DD800 to QSFP-DD800 Active Optical Cable (AOC) that achieves up to 106Gbps data rate per channel through PAM4 modulation. It incorporates an integrated 850nm VCSEL array and PD array within a hot-pluggable QDD800 800G form factor. Operating on a single 3.3V power supply, it maintains a maximum power consumption of 15W per end, and is designed for case operating temperatures from 0°C to 70°C.

Features

- Up to 106Gbps data rate per channel by PAM4 modulation
- Support 800GAUI-8 electrical interface
- Integrated 850nm VCSEL array and PD array
- Hot-pluggable QDD800 800G form factor
- Compliant to QSFP-DD HW Rev6.2
- Compliant with CMIS 4.0
- Single 3.3V power supply
- Maximum power consumption 15W (each end)
- Case operating temperature 0°C to 70°C
- Class 1 laser
- RoHS compliant

Ordering Information

Part Number	Description
V8C-D1DyyyC-AA	800G QSFP-DD800 to QSFP-DD800 AOC, yyy in meters

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Power Supply Voltage	VCC	-0.3	3.6	V	
Control Input Voltage	VI	-0.3	3.465	V	
Relative Humidity (non-condensing)	RH	15	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}			6800	mA	
Sustained peak current at hot plug	I_{CC_SP}			5670	mA	
Maximum Power Dissipation (each end)	P_D			15	W	
Signaling Rate per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate		-100		1000	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	

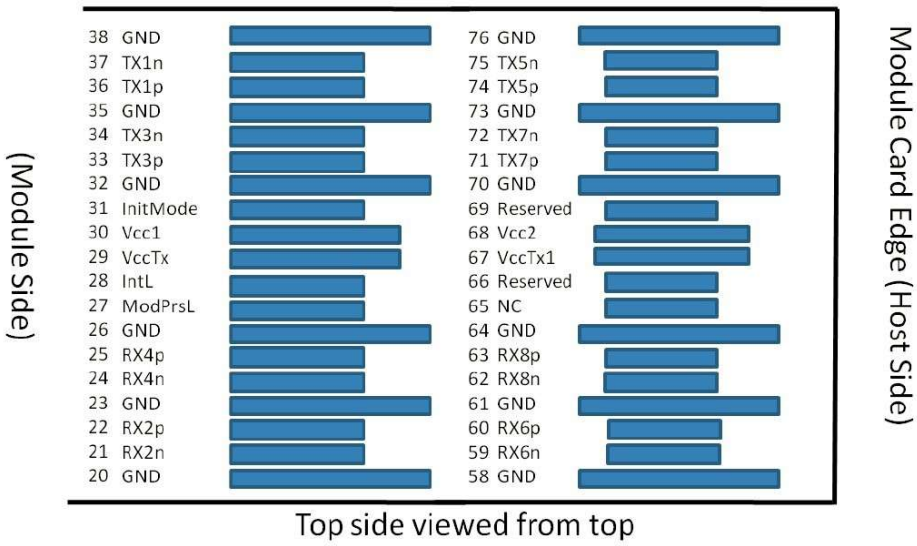
Electrical Specification High Speed Signal

Parameter	Symbol	Min	Typical	Max	Unit	Notes
AC common-mode output Voltage (RMS)				25	mV	
Differential output Voltage (Long mode)				845	mV	
Differential output Voltage (Short mode)				600	mV	
Near-end Eye height, differential		70			mV	
Far-end Eye height, differential		30			mV	
Far end pre-cursor ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	
Pre-FEC BER	BER			1E-6		

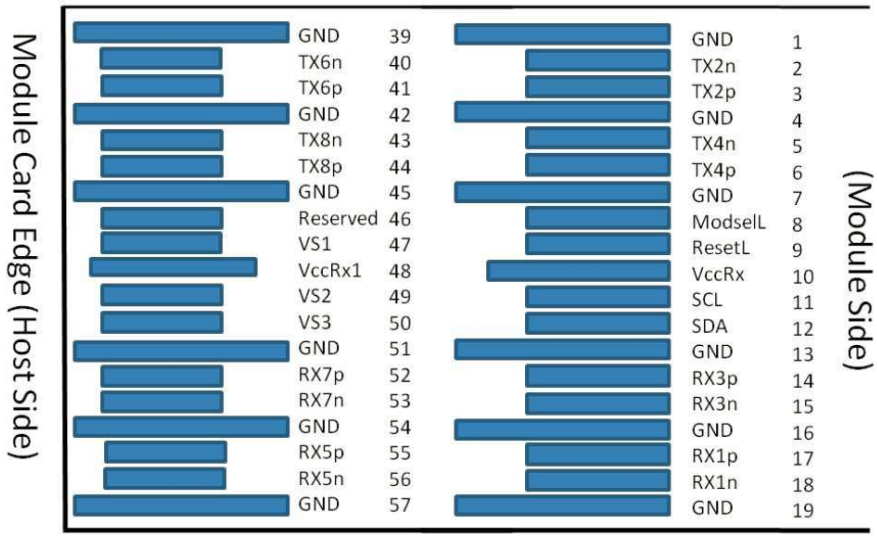
Electrical Specifications Low Speed Signal

Parameter	Symbol	Min	Typical	Max	Unit
Module output SCL and SDA	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	

Electrical Connector Layout



Top side viewed from top



Bottom side viewed from bottom

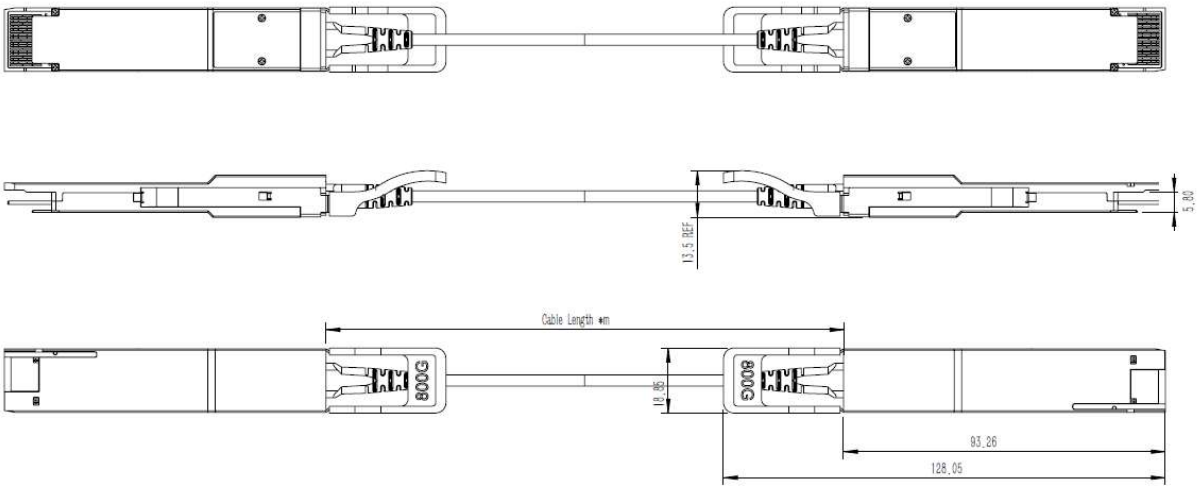
Electrical Pin Definition

Pin #	Logic	Symbol	Description	Pin #	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground

5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS -I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input

34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Mechanical Dimensions



Revision History

Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

For more information

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