800G QSFP-DD to QSFP-DD SR8 AOC
PN: V8C-D1DyyyC-ANA

Product Overview

The V8C-D1DyyyC-ANA is an 800G QSFP-DD to QSFP-DD SR8 Active Optical Cable (AOC) designed for high-density, short-reach connectivity. This hot-pluggable module, in a QSFP-DD form factor, supports an aggregate bit rate of 850 Gb/s. It utilizes a VCSEL transmitter and PIN PD receiver, and complies with IEEE 802.3ck, specifically the 8x100GAUI-1 C2M electrical interface. The module adheres to the QSFP-DD HW Specification Rev 6.3, type 2A housing and supports transmission distances from 0.5m to 50m over OM4 multimode fiber (MMF).

Features

- Support 850Gb/s aggregate bit rate
- Hot-pluggable QSFP-DD form factor • VCSEL transmitter and PIN PD receiver
- Compliant with IEEE 802.3ck: 8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD HW Specification Rev 6.3 type 2A housing
- Support 0.5m~50m transmission with OM4 MMF
- Compliant with CMIS Rev 5.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)

Ordering Information

Part Number	Description
V8C-D1DyyyC-ANA	800G QSFP-DD to QSFP-DD SR8 AOC, yyy in meters

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	85	%	
Data Input Voltage Differential	IVDIP-VDINI		1	V	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	TOPR	0		70	°C	1
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			TBD	mA	
Sustained peak current at hot plug	ICC_SP			TBD	mA	
Maximum Power Dissipation	P_D			TBD	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signalling Speed per Lane	DRL	-	53.125		GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
BER				2E-4		Pre-FEC

Electrical - Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling rate, each lane (range)		53.125 ± 100 ppm			GBd	
Differential pk-pk input Voltage tolerance (TP1a)		750			mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB				 32 80	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5			dB	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common-mode voltage tolerance		-0.35		2.85	V	

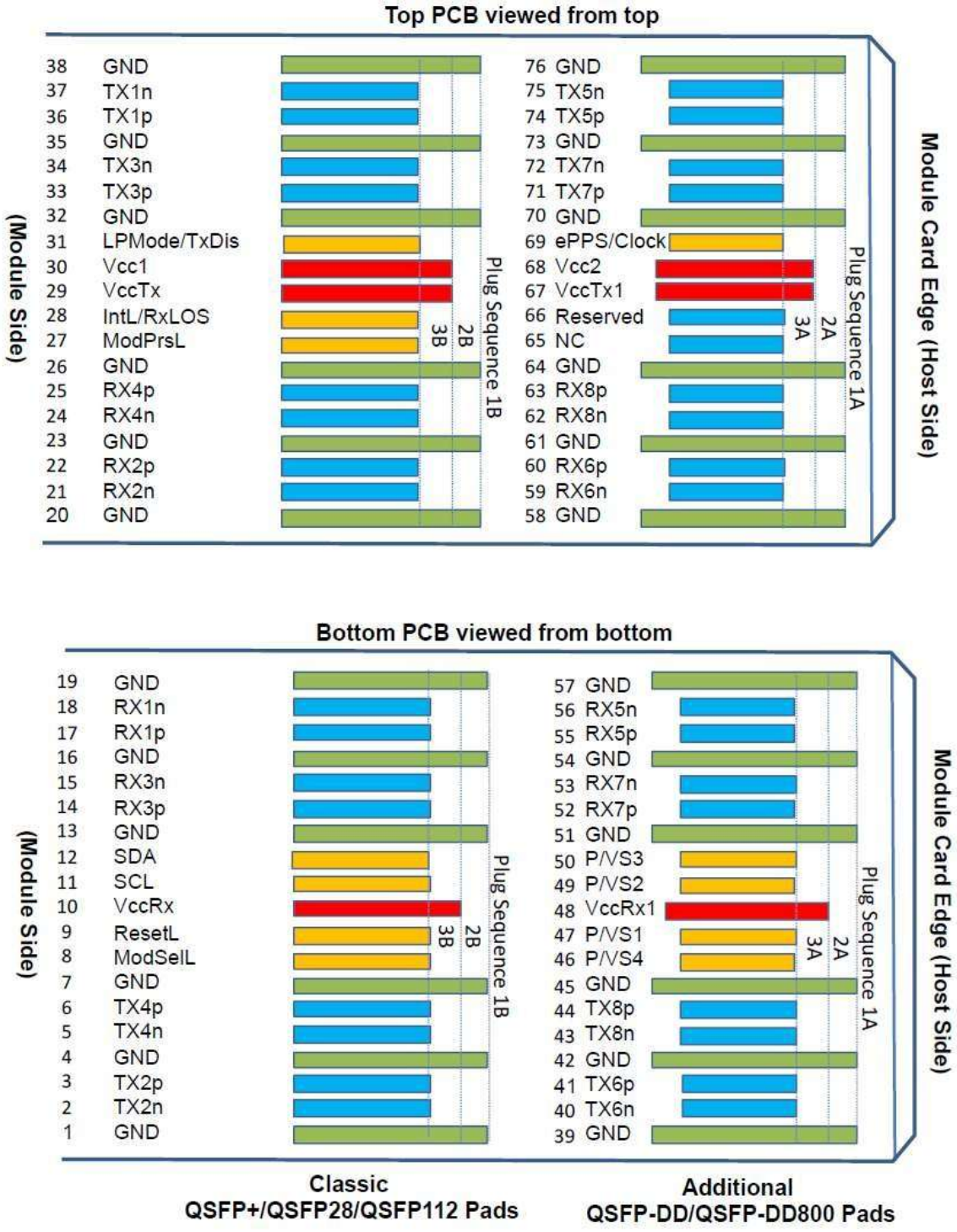
Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling rate, each lane (range)			53.125 ± 100 ppm			GBd
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB				 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode				 600 845	mV	
Eye height	EH	15			mV	
Vertical eye closure	VEC			12	dB	
Common-mode to differential-mode return loss	RLDc		802.3ck 120G-1		dB	
Effective return loss	ERL	8.5			dB	
Differential termination mismatch				10	%	
Transition time		8.5			ps	
DC common-mode voltage tolerance		-0.35		2.85	V	

Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Module output SCL and SDA	V_{OL}	0		0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3		V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7		V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		V_{CC}+0.3	V	
IntL	V_{OL}	0		0.4	V	
	V_{OH}	V_{CC}-0.5		V_{CC}+0.3	V	

Electrical Connector Layout

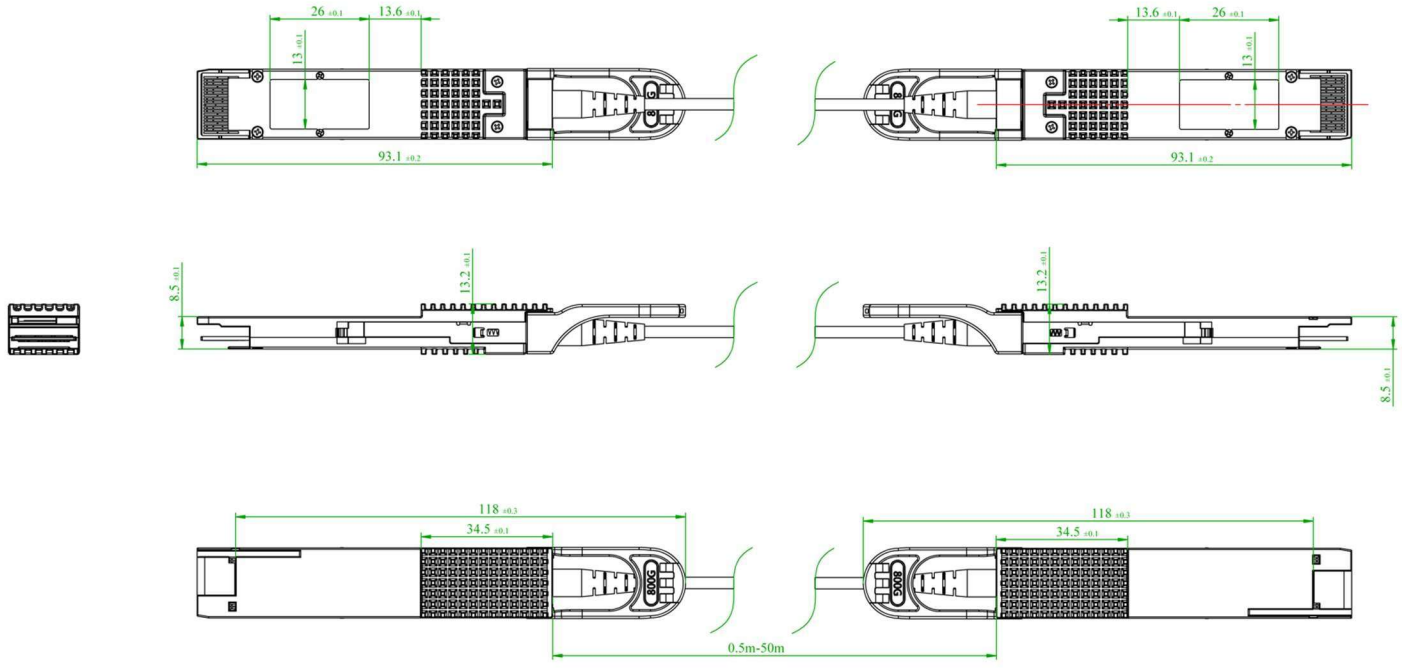


Electrical Pin Definition

Pin #	Logic	Symbol	Description	Pin #	Logic	Symbol	Description
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI serial interface clock	49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS-I/O	SDA	TWI serial interface data	50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	66		Reserved	

29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Mechanical Dimensions



Revision History

Date	Rev	Description
2/1/2025	1.0	Release Version
03/17/2025	1.1	New Template

For more information

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