
800G OSFP800 RHS to OSFP800 RHS AOC

PN: V8C-PIPyC-AR

Product Overview

The V8C-PIPyC-AR is an 800G OSFP800 RHS to OSFP800 RHS active optical cable, delivering up to 106Gbps per channel via PAM4 modulation. It supports the 800GAUI-8 electrical interface and is compliant with OSFP RHS and CMIS Rev 4.0 or above. This cable operates on a single 3.3V power supply, with a maximum power consumption of 15W per end, and is designed for case operating temperatures ranging from 0°C to 70°C.

Features

- Up to 106Gbps data rate per channel by PAM4 modulation
- Support 800GAUI-8 electrical interface
- Compliant with OSFP RHS
- Compliant with CMIS Rev 4.0 or above revision
- Maximum power consumption 15W (each end)
- Single 3.3V power supply
- Case operating temperature 0°C to 70°C
- Compliant to RoHS
- Class 1 laser

Ordering Information

Part Number	Description
V8C-PIPyC-AR	800G OSFP800 RHS to OSFP800 RHS AOC, yyy in meters

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_s	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Control Input Voltage	V_i	-0.3	$V_{CC}+0.5$	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}			6800	mA	
Sustained peak current at hot plug	I_{CC_SP}			5670	mA	
Maximum Power Dissipation (each end)	P_D			15	W	
Signaling Rate per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate		-100		1000	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	

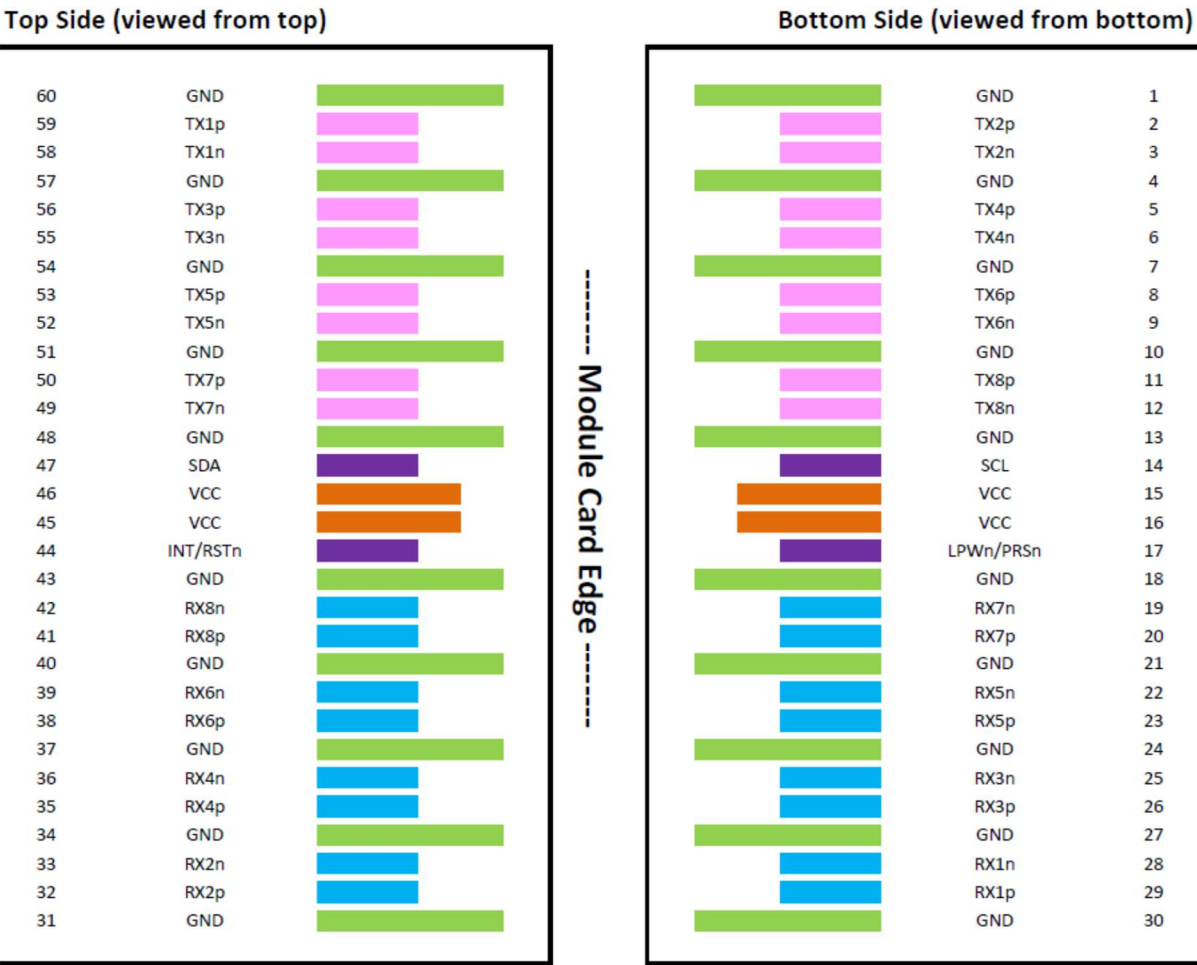
Electrical Specification High Speed Signal

Parameter	Symbol	Min	Typical	Max	Unit	Notes
AC common-mode output Voltage (RMS)				25	mV	
Differential output Voltage (Long mode)				845	mV	
Differential output Voltage (Short mode)				600	mV	
Near-end Eye height, differential		70			mV	
Far-end Eye height, differential		30			mV	
Far end pre-cursor ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	
Pre-FEC BER	BER			1E-6		

Electrical Specifications Low Speed Signal

Parameter	Symbol	Min	Typical	Max	Unit
Module output SCL and SDA	VOL	0	0.4	V	
	VOH	$V_{CC}-0.5$	$V_{CC}+0.3$	V	
Module Input SCL and SDA	VIL	-0.3	$V_{CC}*0.3$	V	
	VIH	$V_{CC}*0.7$	$V_{CC}+0.5$	V	

Electrical Connector Layout



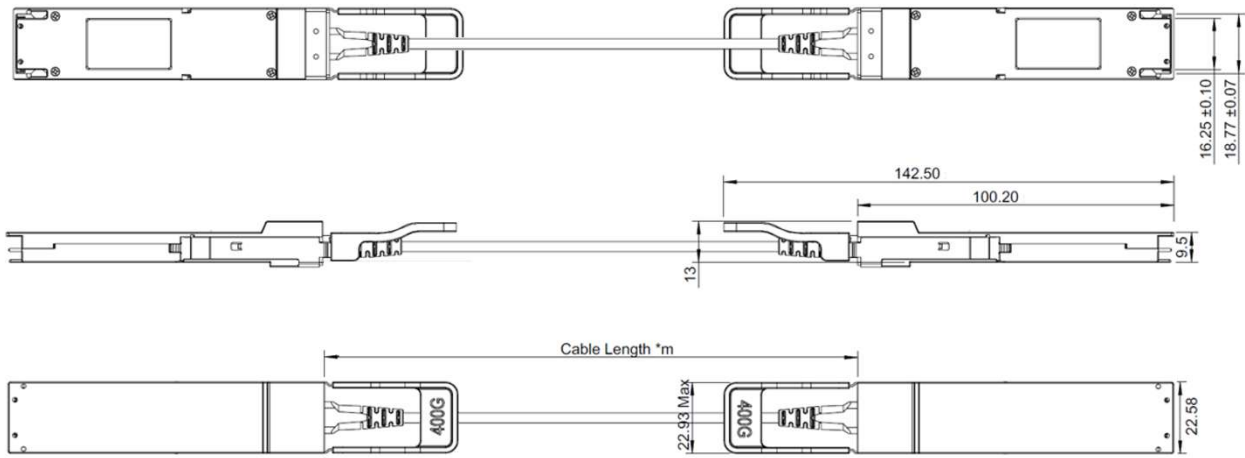
Electrical Pin Definition

Pin#	Logic	Symbol	Description	Direction	Plug	Notes
1		GND	Ground		1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	Input from Host	3	
3	CML-I	TX2n	Transmitter Data Inverted	Input from Host	3	
4		GND	Ground		1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	Input from Host	3	
6	CML-I	TX4n	Transmitter Data Inverted	Input from Host	3	
7		GND	Ground		1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	Input from Host	3	
9	CML-I	TX6n	Transmitter Data Inverted	Input from Host	3	
10		GND	Ground		1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	Input from Host	3	
12	CML-I	TX8n	Transmitter Data Inverted	Input from Host	3	
13		GND	Ground		1	

14	LVC MOS-I/O	SCL	2-wire Serial interface clock	Bi-directional	3	
15		VCC	+3.3V Power	Power from Host	2	
16		VCC	+3.3V Power	Power from Host	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	3	
18		GND	Ground		1	
19	CML-O	RX7n	Receiver Data Inverted	Output to Host	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	Output to Host	3	
21		GND	Ground		1	
22	CML-O	RX5n	Receiver Data Inverted	Output to Host	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	Output to Host	3	
24		GND	Ground		1	
25	CML-O	RX3n	Receiver Data Inverted	Output to Host	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	Output to Host	3	
27		GND	Ground		1	
28	CML-O	RX1n	Receiver Data Inverted	Output to Host	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	Output to Host	3	
30		GND	Ground		1	
31		GND	Ground		1	
32	CML-O	RX2p	Receiver Data Non-Inverted	Output to Host	3	
33	CML-O	RX2n	Receiver Data Inverted	Output to Host	3	
34		GND	Ground		1	
35	CML-O	RX4p	Receiver Data Non-Inverted	Output to Host	3	
36	CML-O	RX4n	Receiver Data Inverted	Output to Host	3	
37		GND	Ground		1	
38	CML-O	RX6p	Receiver Data Non-Inverted	Output to Host	3	
39	CML-O	RX6n	Receiver Data Inverted	Output to Host	3	
40		GND	Ground		1	
41	CML-O	RX8p	Receiver Data Non-Inverted	Output to Host	3	
42	CML-O	RX8n	Receiver Data Inverted	Output to Host	3	
43		GND	Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	3	
45		VCC	+3.3V Power	Power from Host	2	
46		VCC	+3.3V Power	Power from Host	2	
47	LVC MOS-I/O	SDA	2-wire Serial interface data	Bi-directional	3	
48		GND	Ground		1	
49	CML-I	TX7n	Transmitter Data Inverted	Input from Host	3	
50	CML-I	TX7p	Transmitter Data Non-Inverted	Input from Host	3	
51		GND	Ground		1	
52	CML-I	TX5n	Transmitter Data Inverted	Input from Host	3	
53	CML-I	TX5p	Transmitter Data Non-Inverted	Input from Host	3	
54		GND	Ground		1	
55	CML-I	TX3n	Transmitter Data Inverted	Input from Host	3	

56	CML-I	TX3p	Transmitter Data Non-Inverted	Input from Host	3	
57		GND	Ground		1	
58	CML-I	TX1n	Transmitter Data Inverted	Input from Host	3	
59	CML-I	TX1p	Transmitter Data Non-Inverted	Input from Host	3	
60		GND	Ground		1	

Mechanical Dimensions



Revision History

Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

For more information

Vitex LLC
32 Mercer St.
Hackensack, NJ 07601

(201) 296-0145
info@vitextech.com
www.vitextech.com

