

800G OSF800P to 4xOSFP 200G IB DAC

PN: V8C-P4PyyC-ENA

Product Overview

The V8C-P4PyyC-ENA is an 800G OSFP800 to 4xOSFP 200G InfiniBand Direct Attach Copper (DAC) breakout cable, designed to comply with the OSFP MSA. It supports transmission data rates up to PAM4 106.25Gbps per channel, enabling 800Gb/s transmission. This cable is equipped with built-in EEPROM functions and operates within a case temperature range of 0°C to +70°C.

Features

- OSFP Module compliant to OSFP MSA
- Transmission data rate up to PAM4 106.25Gbps per channel
- Enable 800Gb/s Transmission
- Built-in EEPROM functions
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

OSFP-TYPE 2



OSFP-RHS



Ordering Information

Part Number	Description
V8C-P4PyyC-ENA	800G OSF800P to 4xOSFP 200G IB DAC, yyy in meters



Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Storage temperature	Ts	-40		85	°C
Operating Case temperature	Tc	0		70	°C
Humidity	Rh	5		85	%
Data Rate			800		Gbps

Physical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Length	L	1		3.0	M	
AWG		28		25	AWG	
Jacket material		HAIRTAIL+ Technology Net, Gray				

Electrical Specifications

Parameter	Symbol	Min	Typical	Max		Unit
Resistance	Rcon			3		ohm
Insulation Resistance	Rins			10		Mohm
Raw cable impedance	Zca	95	100	110		ohm
Mated connector Impedance	Zmated	85	100	115		ohm
Maximum insertion loss at 26.56 GHz	SDD21	11		18	1.5M	dB
				19.75	2.0M	
				25.3	3.0M	
Differential to common-mode return loss	SCD11/22	$RL_{cd}(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$ For 0.05 ≤ f ≤ 40 GHz, Where f is the frequency in GHz				dB
Differential to common-mode conversion loss	SCD21-SDD21	$Conversion_loss(f) - IL(f) \geq \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases}$ For 0.05 ≤ f ≤ 40 GHz, Where f is the frequency in GHz				dB

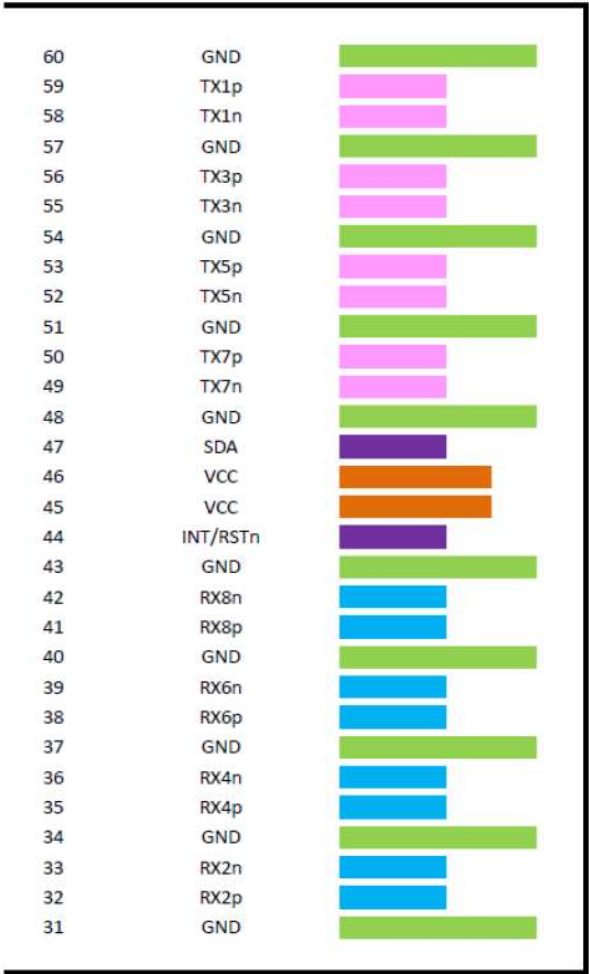


Common-mode to common-mode return loss	SCC11/22	$RL_{cc}(f) \geq 1.8$ For $0.05 \leq f \leq 40$ GHz, Where f is the frequency in GHz			dB
Minimum COM	COM	3			dB
Minimum cable assembly ERL ^a	ERL	8.25			dB

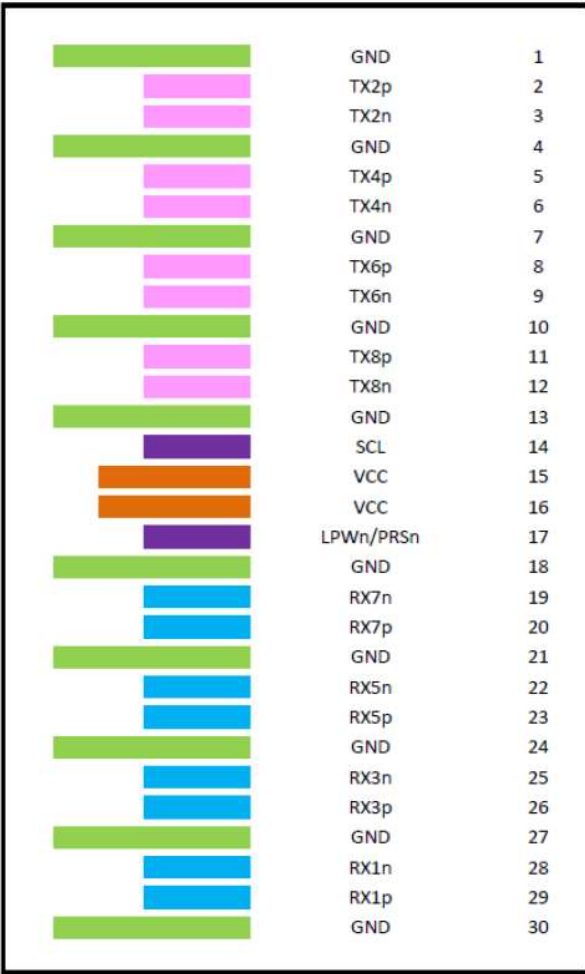
a . Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

Electrical Connector Layout

Top Side (viewed from top)



Bottom Side (viewed from bottom)

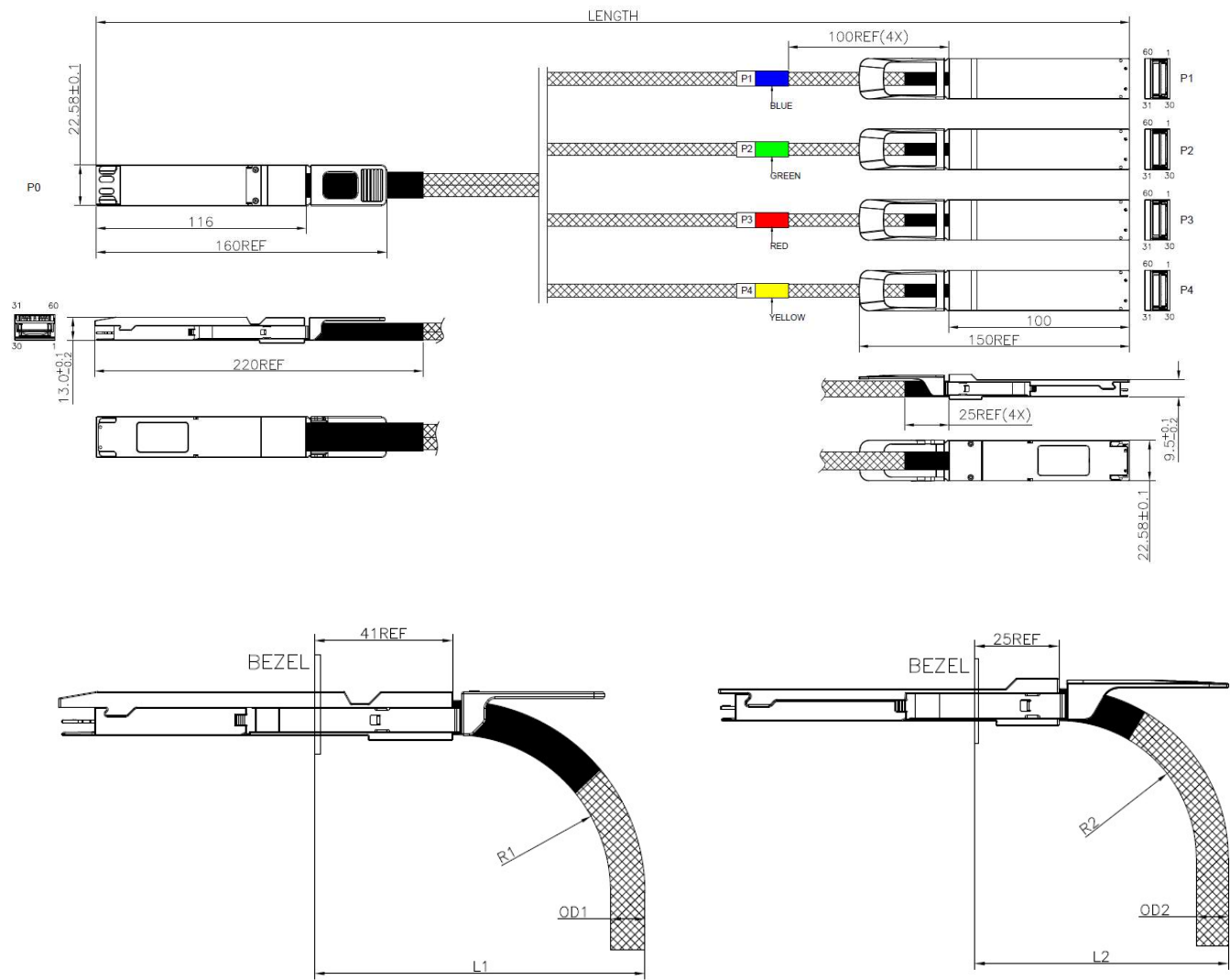


Electrical Pin Definition

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Mechanical Dimensions



Bending radius

Wire gauge	OD1(Ref)	Min. bend radius (R1)	Min. Bend space(L1)	OD2 (Ref)	Min. bend radius (R2)	Min. Bend space(L2)
25AWG	13.0mm	40mm	95mm	7.0mm	25mm	60mm



Revision History

Date	Rev	Description
2/1/2024	1.0	Release Version
03/17/2025	1.1	New Template

For more information

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