2x100G QSFP-DD LAN-WDM transceiver
PN: VD-2CLR4CC-AA

Product Overview

Vitex VD-2CLR4CC-AA is designed for use in 200G Ethernet links over 10km single mode fiber. The implementation of an 8 channel DML TOSA and ROSA is used to create a Dual LAN-WDM transceiver. The QSFP-DD 2x100G LAN-WDM transceiver is characterized by an 8x25G NRZ electrical interface and Dual CS connectors and is compliant with QSFP-DD MSA standards.

Features

- Supports 206Gbps
- Single 3.3V Power Supply
- Power dissipation < 8.0W
- Up to 10km over SMF
- QSFP-DD MSA Compliant
- 8x25G electrical interface
- Dual CS connector
- Commercial case temperature range of 0°C to 70°C
- 8*25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- I2C interface with integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA*1
- RoHS compliant

Applications

- QSFP-DD 2x100G Ethernet
- Data Center

Ordering Information

Part Number	Description
VD-2CLR4CC-AA	200G QSFP-DD 2x100G-LR4, 10km SMF, 1310 nm, Dual-CS, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Storage Temperature	Ts	-40		+85	℃	
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Data Input Voltage – Single Ended		-0.5		Vcc+0.5	V	
Data Input Voltage – Differential				0.8	V	1
Operating Relative Humidity	RH	5		85	%	
Receiver Damage Threshold, per Lane	Rxdmg	5.5			dBm	
Operating case temperature	Tc	0	25	70	ºC	2
Power supply voltage	Vcc	3.135	3.3	3.465	V	
Power dissipation	PD			8	W	
Electrical Signal Rate per Channel			25.78125		GBd	3
Optical Signal Rate per Channel			25.78125		GBd	4
Power Supply Noise				66	mVpp	5
Receiver Differential Data Output Load		100			Ohm	

Exceeding any one of these values may damage the device permanently.

1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600 mV peak to peak differential.
2. The position of case temperature measurement is shown in Figure 9.
3. CAUI-4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
4. 2x100G LR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
5. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 7 for recommended power supply filter.

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling speed per lane	BRAVE		25.78125		Gbps	
Data Rate Variation		-100		+100	ppm	
Modulation format			NRZ			
Lane_0/4 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane_1/5 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane_2/6 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane_3/7 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Total Average Output Power	Po			10.5	dBm	
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	4			dB	
Average Launch Power each Lane	Peach	-4.3		4.5	dBm	1
Transmit OMA each Lane	TxOMA	-1.3		4.5	dBm	2
Launch power in OMA minus TDP, each lane	OMA-TDP	-2.3			dBm	
Transmitter and Dispersion Penalty per Lane	TDP			2.2	dB	3
Average launch power of OFF transmitter				-30	dBm	

Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	4
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					5

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDP < 1.0dB, the OMA (min) must exceed this value.
3. TDP does not include a penalty for multi-path interference (MPI).
4. Transmitter reflectance is defined looking into the transmitter.
5. Hit ratio of $5x10^{-5}$

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Signaling Speed per Lane	BRAVE		25.78125		Gbps	
Data Rate Variation		-100		+100	ppm	
Lane 0/4 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane 1/5 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane 2/6 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane 3/7 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Damage threshold	Rxdmg	5.5			dBm	
Average receive power each lane	Rxpow	-10.6		4.5	dBm	1
Receive Power (OMA) per Lane	RxOMA			4.5	dBm	
Unstressed Receiver Sensitivity (OMA) per Lane	Rxsens			-8.6	dBm	2
Stressed Receiver Sensitivity (OMA) per Lane	RXSRS			-6.8	dBm	3
Vertical Eye Closure Penalty	VECP	1.8			dB	4
Stressed J2 Jitter	J2	0.3			UI	4
Stressed J9 Jitter	J9	0.47			UI	4
LOS Assert	LOSA	-25			dBm	
LOS De-Assert	LOSD			-15	dBm	
LOS Hysteresis		0.5			dB	
RSSI accuracy		-3		+3	dB	
Receiver reflectance				-26	dB	

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Receiver sensitivity (OMA), each lane (max) is informative.
3. Measured with conformance test signal at TP3 for BER = 10^{-12}.
4. Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical – Receiver

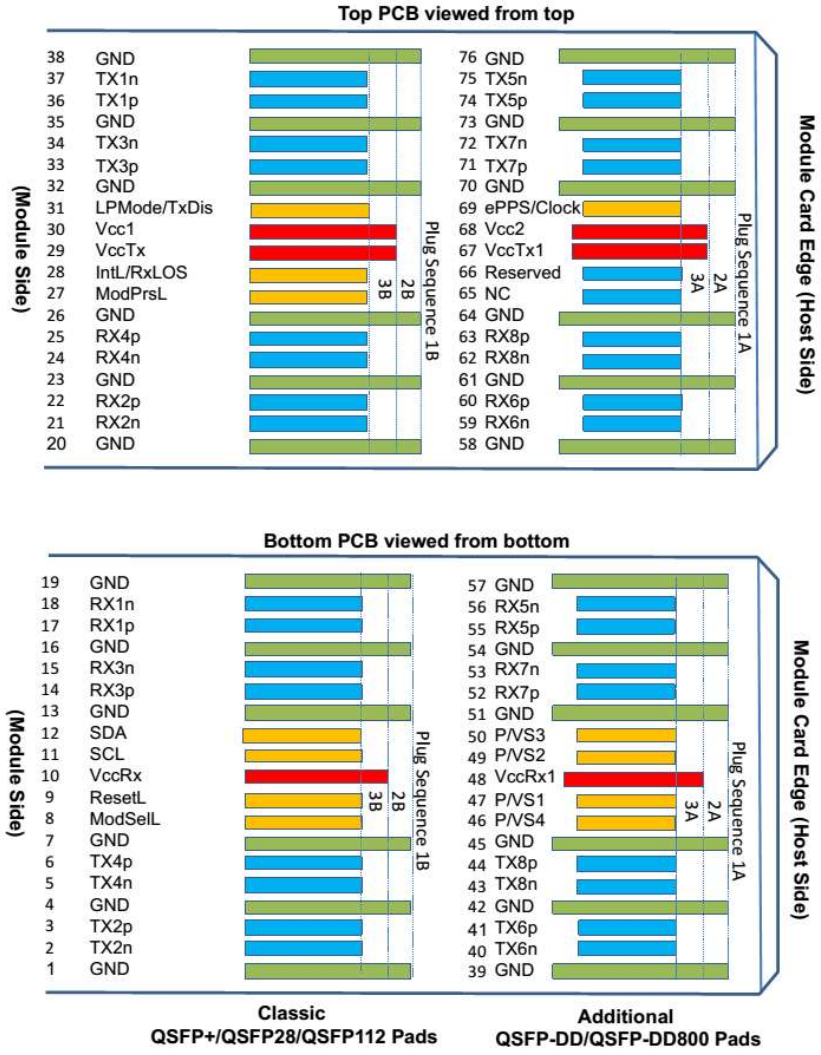
Parameter	Symbol	Min	Typical	Max	Unit	
Transceiver Power Consumption				8	W	
Transceiver Power Supply Current, Total				2560	mA	
Signaling Rate, Per Lane	TP1		25.78125		GBd	+/-100ppm
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Differential Return Loss(min)	TP1		Equation(83E-5)		dB	802.3bm
Differential to common mode input return loss (min)	TP1		Equation(83E-6)		dB	802.3bm
Differential termination mismatch	TP1			10	%	
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode output voltage	TP1	-350		2850	mV	1
Module stressed input test	TP1a					2
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter			Table 88-13			802.3bm
Eye height		95			mV	

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
2. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit
Signaling Rate, Per Lane(range)	TP4		25.78125 ± 100 ppm		GBd
Differential output voltage	TP4			900	mV
Differential output return loss (Min)	TP4		Equation (83E-2)	dB	
Differential to common mode conversion return loss (min)	TP4		Equation (83E-3)	dB	
Differential termination mismatch	TP4			10	%
Common mode voltage	TP4	-0.35		2.85	V
Transition Time (20% to 80%)	TP4	12			ps
Eye width	TP4	0.57			UI
Eye height differential	TP4	228			mV
Vertical eye closure	TP4			5.5	dB

Electrical Connector Layout



Electrical Pin Definition

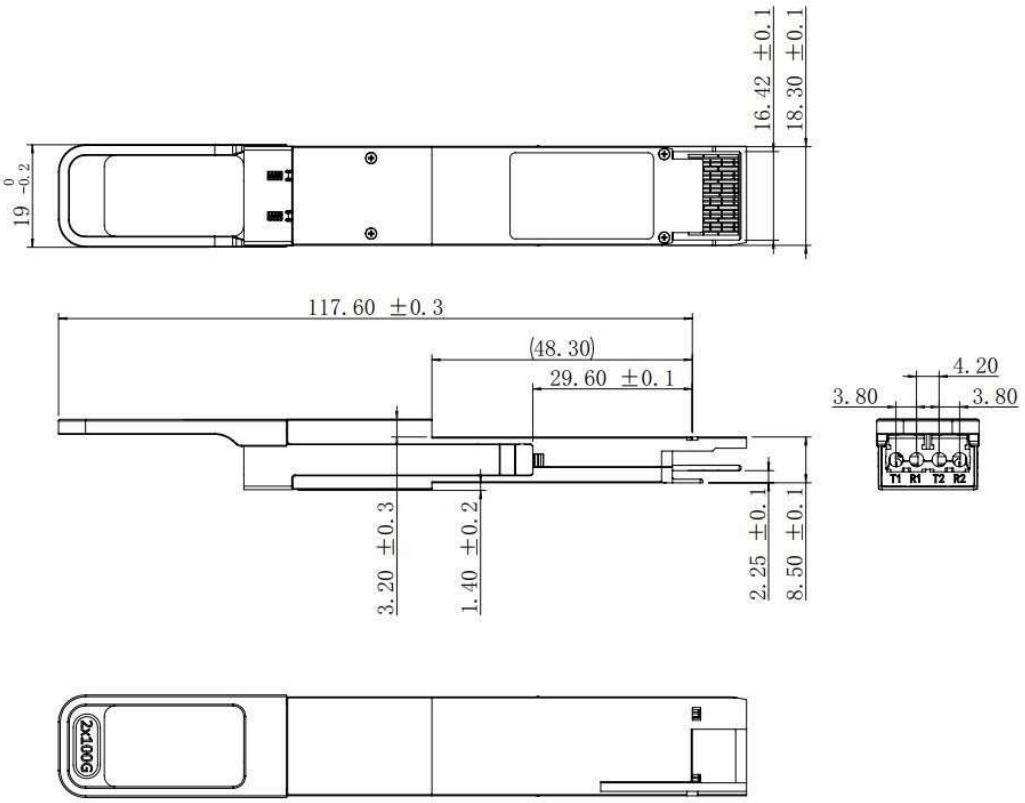
PIN #	Logic	Symbol	Description	Plug Sequence	Remarks
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModselL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	

10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-C	Rx3p	Receiver Non-inverted Data Output	3B	
15	CML-C	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-C	Rx1p	Receiver Non-inverted Data Output	3B	
18	CML-C	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-C	Rx2n	Receiver Non-inverted Data Output	3B	
22	CML-C	Rx2p	Receiver Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-C	Rx4n	Receiver inverted Data Output	3B	
25	CML-C	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non—Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non—Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML-I	P/VS4	Module Vendor Specific 4	3A	3
47	LVCMOS/CML-I	P/VS4	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-I	P/VS2	Module Vendor Specific 2	3A	3
50	LVCMOS/CML-I	P/VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-inverted Data Output	3A	

56	CML-O	Rx5n	Receiver inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	Epps/Clock	1PPS PTP clock or reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFPDD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a maximum current of 500 mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in QSFP-DD MSA. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequences 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
5. Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10k ohms.
6. Epps/Clock If not used recommended to be terminated with 50ohms to ground on the host.

Mechanical Dimensions



Revision History

Date	Rev	Description
09/28/2022	1.0	Initial Release
09/13/2023	1.1	Power dissipation CALIX ONLY update
02/17/25	2.0	

For more information

Vitex LLC 32 Mercer St
Hackensack, NJ 07601

(201) 296-0145
info@vitextech.com
www.vitextech.com