200G QSFP-DD 20km Optical Transceiver
PN: VD-2CLR4CP-EA

Product Overview

Vitex's VD-2CLR4CP-EA is a Pluggable, Parallel, Fiber-Optic QSFP Double Density for 200 Gigabit Ethernet Applications. This transceiver is a high-performance module for multi-lane data communication and interconnection applications. These modules are designed to operate over single mode fiber systems using a nominal wavelength of 1310nm. Each lane can operate at 53.125Gbps up to 20km using G.652 SMF with KP-FEC.

Features

- 4x53.125Gbps(26.5625GBd) PAM4 parallel optics architecture
- 8x25.78125Gbps NRZ retimed electrical I/O
- 4x53Gbps PAM4 transmitter and PAM4 receiver
- 4 channels 1310nm cooled EML transmitter
- 4 channels PIN photo detector array receiver
- Internal 8:4 Gearbox with KP4 FEC circuits on both receiver and transmitter channels
- Power consumption <8.5W
- Hot Pluggable QSFP DD form factor and Compliant with CMIS 4.0
- Maximum link length of 20km G.652 SMF with KP-FEC
- MPO12 APC connector receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0 °C to 70°C
- 3.3V power supply voltage
- RoHS compliant (lead free)

Applications

- IEEE 802.3bs 200GBASE-DR4

Ordering Information

Part Number	Description
VD-2CLR4CP-EA	200G QSFP28-DD, PSM4 20km SMF, 1310nm, MPO16, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage (Maximum)	Vcc	-0.3		3.6	V
Input Voltage	Vin	-0.3		Vcc+0.3	V
Storage Temperature	Tst	-20		85	°C
Case Operating Temperature	Top	0		70	°C
Humidity(non-condensing)	Rh	5		95	%
Supply Voltage (Recommended)	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	°C
Signal Rate per Electrical Channel(8x25G)			25.78125		Gbps
Signal Rate per Optical Channel (4x53G)			53.125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			8.5	W

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	λc	1304.5		1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane	Pout	-4.1		4	dBm	
Optical Modulation Amplitude (OMAouter), each lane	OMA	-2		3.8	dBm	
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			3.4	dB	
Extinction Ratio	ER	3.5			dB	
Average launch power of OFF transmitter, each lane				-30	dB	

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Centre Wavelength	λc	1304.5		1317.5	nm	
Receiver Sensitivity in OMAouter	RXsen		-10	-9	dBm	1
Average power at receiver, each lane input, each lane	Pin	-9		4	dBm	
Receiver Reflectance				-12	dB	
LOS Assert			-13.5		dBm	
LOS De-Assert – OMA			-12		dBm	
LOS Hysteresis		0.5			dB	

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential Output Impedance	Zout	90	100	110	ohm	
Differential Output Voltage Amplitude	ΔVout			1100	mVp-p	1

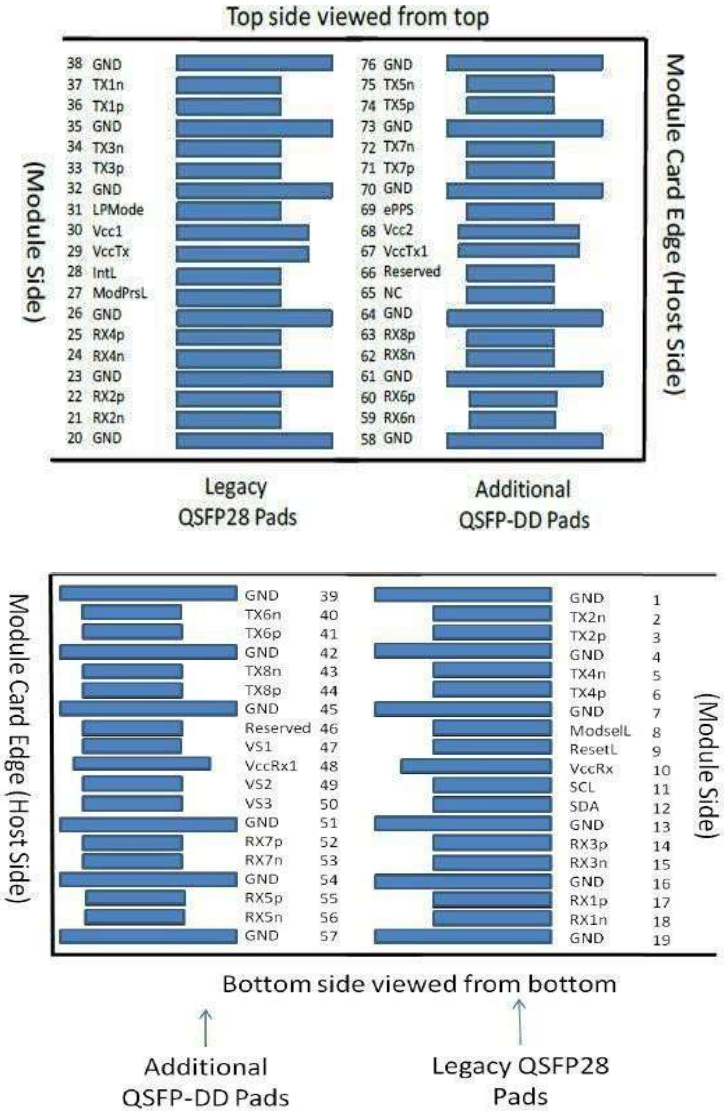
1. Differential output voltage amplitude is measured between RxnP and RxnN.

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential Input Impedance	Zin	90	100	110	ohm	
Differential Input Voltage Amplitude	ΔVin	900		1200	mVp-p	1

1. Differential input voltage amplitude is measured between TxnP and TxnN.

Electrical Layout



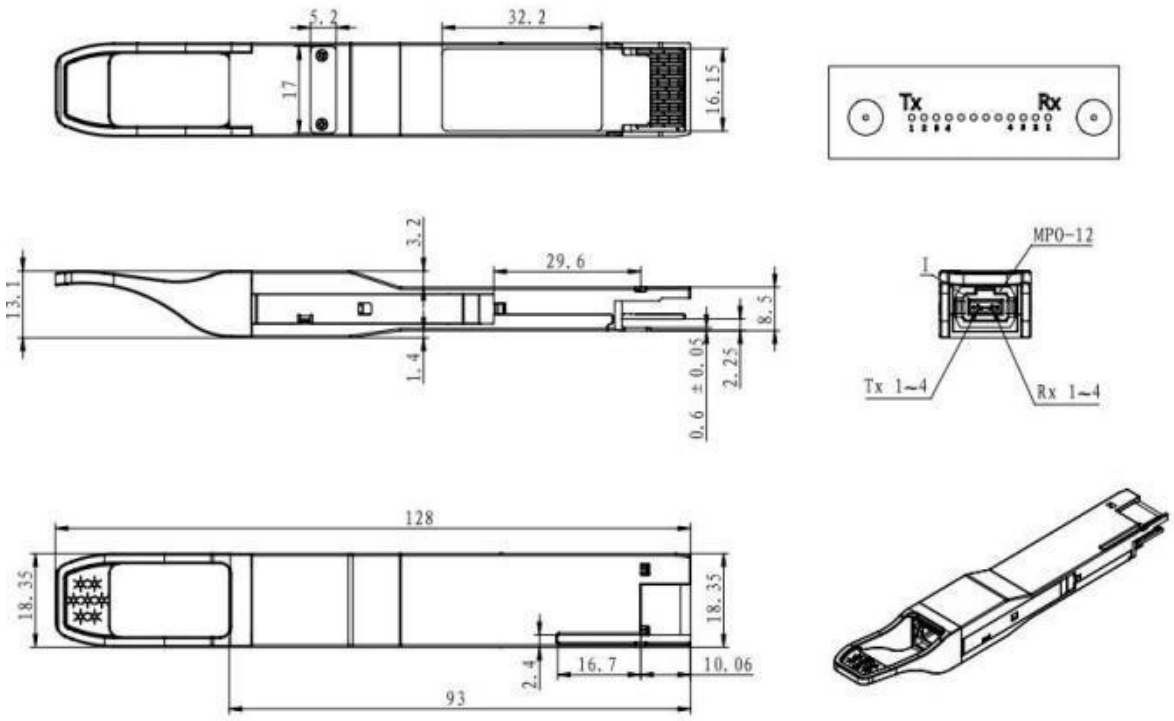
Electrical Pin Definition

PIN #	Logic	Symbol	Description	Remarks
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModselL	Module Select	
9	LVTTL-1	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-C	Rx3p	Receiver Non-inverted Data Output	
15	CML-C	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-C	Rx1p	Receiver Non-inverted Data Output	
18	CML-C	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-C	Rx2n	Receiver Non-inverted Data Output	
22	CML-C	Rx2p	Receiver Inverted Data Output	
23		GND	Ground	1
24	CML-C	Rx4n	Receiver inverted Data Output	
25	CML-C	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non—Inverted Data Input	
42		GND	Ground	1

43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non—Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-inverted Data Output	
56	CML-O	Rx5n	Receiver inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver inverted Data Output	
60	CML-O	Rx6p	Receiver Non-inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver inverted Data Output	
63	CML-O	Rx8p	Receiver Non-inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) referenceclock input	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are comon within the QSFP-DD module and all module voltages are referenced to this po-te-nial unless otherwise noted. Connect these directly to the host board signal- common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated within 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.

Mechanical Dimensions



Revision History

Date	Rev	Description
10/1/2021	1.0	Initial Release
05/17/2023	1.1	Updated Format and specification
02/17/2025	2.0	New branding guidelines

For more information

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