200G QSFP-DD LR8 Optical Transceiver
PN: VD-2CLR8CP-EA

Product Overview

VD-2CLR8PS-EA is an Eight-Channel, Pluggable, Fiber-Optic QSFP DD LR8 for 2 × 100 Gigabit Ethernet Applications. It integrates eight data lanes in each direction with 208Gbps bandwidth. Each lane can operate at 26Gbps up to 20km over G.652 single mode fiber. The electrical interface uses a 76-contact edge type connector. The optical interface uses a 16 fiber MTP(MPO) connector.

Features

- 8 channels full-duplex transceiver modules
- Supports 8x25Gb/s aggregate bit rates
- Supports 8x10Gb/s aggregate bit rates if required
- 8 channels 1310nm DFB
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <6.5W
- Hot Pluggable QSFP DD form factor
- Up to 20km reach for G.652 SMF
- Single male MPO16(APC 8-degree) connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant (lead free)

Applications

- 2×100G Ethernet links
- Infiniband DDR/EDR
- Datacenter and Enterprise networking

Ordering Information

Part Number	Description
VD-2CLR8CP-EA	200G QSFP28-DD LR8, 20km SMF, 1310nm, MPO16, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage (Maximum)	Vcc	-0.3		3.6	V
Input Voltage	Vin	-0.3		Vcc+0.3	V
Storage Temperature	Ts	-20		85	°C
Case Operating Temperature	Tc	0		70	°C
Humidity(non-condensing)	Rh	5		95	%
Supply Voltage (Recommended)	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	°C
Data Rate Per Lane	fd	10.3125	25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		5.8	6.5	W
Fiber Bend Radius	Rb	0.002		20	km

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λc	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power (each lane)	PAVG	-4		4	dBm	
Optical Modulation Amplitude (each lane)	POMA	-3.7		4.3	dBm	
TDP,each lane	TDP			2.9	dB	
Extinction Ratio	ER	3.5			dB	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Average Launch Power of OFF Transmitter (each lane)	POFF			-30	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	{0.31,0.4,0.45,0.34,0.38.0.4} Hit Ratio = $5x10^{-5}$					

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λc	1295	1310	1325	nm	
Damage Threshold, each lane	THd	5.0			dBm	
Average Receive Power each lane		-15		4.0	dBm	
Receive power, each lane (OMA) (max)				4.3	dBm	
Receiver Reflectance	RR			-26	dBm	
Receiver Sensitivity (OMA) each lane	SEN			-11	dBm	3
Receiver Sensitivity (OMA) each lane,	SEN			-11.5	dBm	4
LOS Assert	LOSA			-16	dBm	
LOS De-Assert	LOSD			-14	dBm	
LOS Hysteresis	LOSH	0.5		3	dB	

1. Even if the TDP<1dB, the OMA min must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Sensitivity is specified at 1E-12 BER at 25.78125Gb/s.
4. Sensitivity is specified at 1E-12 BER at 10.3125Gb/s.

Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential Output Impedance	Zout	90	100	110	ohm	
Differential Output Voltage Amplitude	ΔVout	300		850	mVp-p	1
Output Logic Level High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level Low	VOL	0		0.4	V	

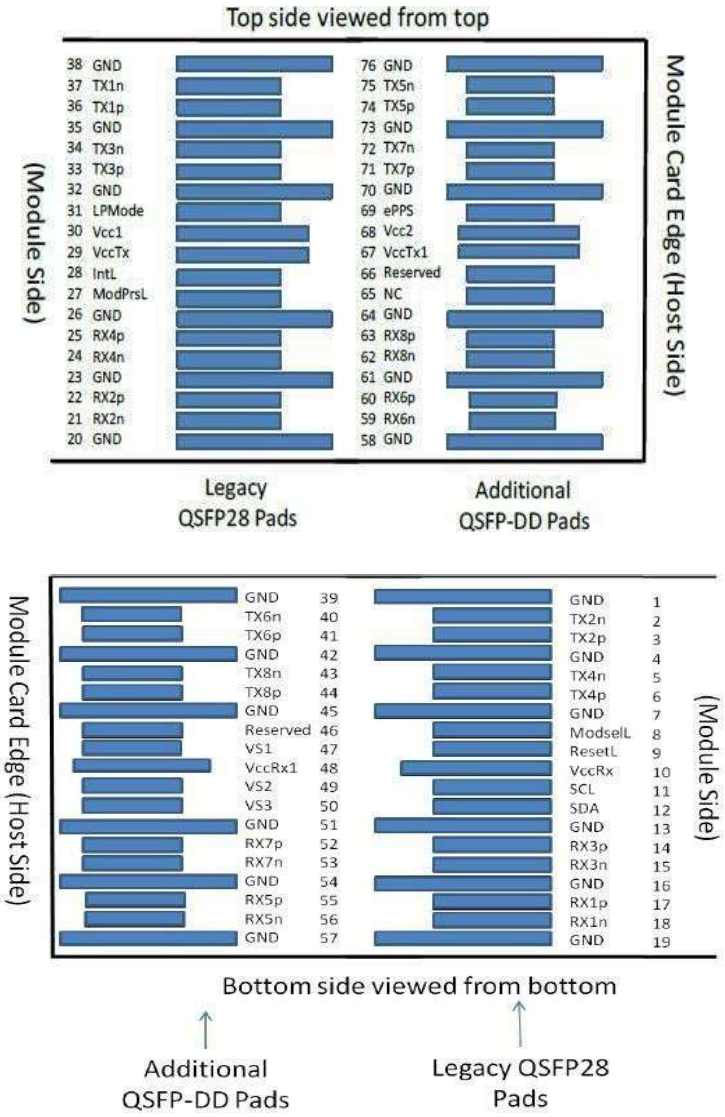
1. Differential output voltage amplitude is measured between RxnP and RxnN.

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential Input Impedance	Zin	90	100	110	ohm	
Differential Input Voltage Amplitude	ΔVin	190		700	mVp-p	1
Input Logic Level High	VIH	2.0		Vcc	V	
Input Logic Level Low	VIL	0		0.8	V	

1. Differential input voltage amplitude is measured between TxnP and TxnN.

Electrical Layout



Electrical Pin Definition

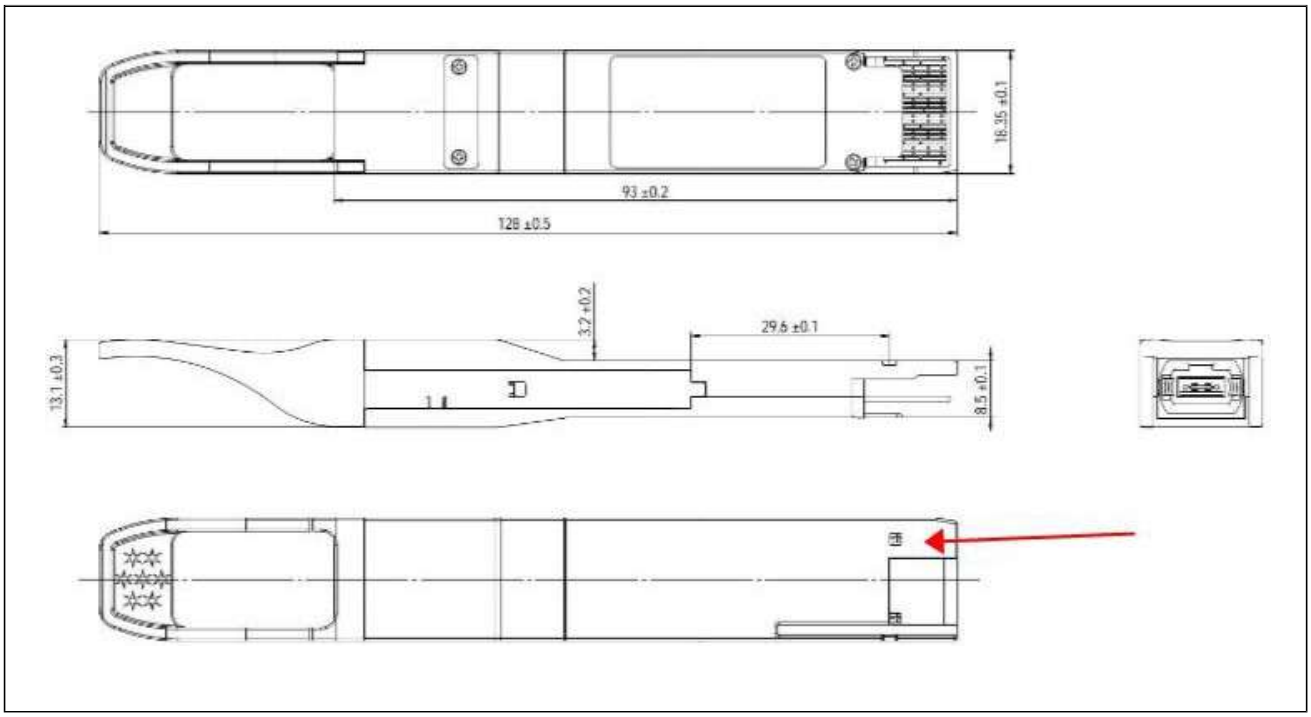
PIN #	Logic	Symbol	Description	Remarks
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModselL	Module Select	

9	LVTTL-1	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-C	Rx3p	Receiver Non-inverted Data Output	
15	CML-C	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-C	Rx1p	Receiver Non-inverted Data Output	
18	CML-C	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-C	Rx2n	Receiver Non-inverted Data Output	
22	CML-C	Rx2p	Receiver Inverted Data Output	
23		GND	Ground	1
24	CML-C	Rx4n	Receiver inverted Data Output	
25	CML-C	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non—Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non—Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1

52	CML-O	Rx7p	Receiver Non-inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-inverted Data Output	
56	CML-O	Rx5n	Receiver inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver inverted Data Output	
60	CML-O	Rx6p	Receiver Non-inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver inverted Data Output	
63	CML-O	Rx8p	Receiver Non-inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are comon within the QSFP-DD module and all module voltages are referenced to this po-te-nial unless otherwise noted. Connect these directly to the host board signal- common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated within 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.

Mechanical Dimensions



Revision History

Date	Rev	Description
10/1/2021	1.0	Initial Release
05/17/2023	1.1	Updated Format and specification
02/17/2025	2.0	New branding guidelines

For more information

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