400G QSFP56-DD LR4 Optical Transceiver

PN: VD-4CLR4CS-AA

Product Overview

Vitex VD-4CLR4CS-AA is designed for 400G optical connections of up to 10km. The transceiver is a fully integrated optical transceiver modulated using a 4-level pulse amplitude modulation (PAM4) format that transmits at a data rate of 425Gbps over 4 lanes on CWDM wavelength grids, running at 106.25 Gbps each. They are compliant with the QSFP-DD MSA and 400GBASE-LR4-10 standards.

Features

- Compliant with 400G-LR4-10 optical specifications
- Compliant with QSFP-DD MSA
- Compliant with CMIS4.0 Management interface specifications
- Duplex LC receptacles
- 4 x 106.25Gbps PAM4 cooled EML
- 8 x 53.125Gbps PAM4 electrical interface
- Transmission distance up to 10km
- Single 3.3V power supply
- Power dissipation <8W
- Commercial operating temperature: 0℃ to +70℃
- RoHS Compliant

Applications

- 400G BASE-LR4 Ethernet

Ordering Information

Part Number	Description
VD-4CLR4CS-AA	400G QSFP56-DD LR4, 10km SMF, 1310nm, Duplex LC, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	15		85	%	
Supply Voltage (Maximum)	V_{CC}	-0.5		3.6	V	
Supply Voltage (Recommended)	V_{CC}	3.13	3.3	3.47	V	
Operating Case Temperature	TC	0		70	°C	
Data Rate PER Channel			53.125 ±100ppm		GBd	
Modulation Format			PAM4			

Optical – Transmitter

Parameter		Symbol	Min	Typical	Max	Unit	Remarks
Lane wavelengths		λ	1264.5		1277.5	nm	1
			1284.5		1297.5		
			1304.5		1317.5		
			1324.5		1337.5		
Side-mode suppression ratio		SMSR	30			dB	
Total Average launch power		Pr			10	dBm	
Average launch power, each lane		P	-1.4		4.5	dBm	
Outer Optical Modulation Amplitude, each lane	For TDECQ < 1.4dB	OMAouter	0.3		4.4	dBm	
	For 1.4 < TDECQ <3.9dB		-1.1+ TDECQ		4.4	dBm	
Difference in launch power between any two lanes (OMA outer)					4	dB	
Transmitter and dispersion eye closure for PAM4(TDEVQ), each lane		TDECQ			3.9	dB	
Transmitter eye closure for PAM4(TECQ), each lane		TECQ			3.9	dB	
| TDECQ-TECQ |					2.5	dB	
Extinction Ratio		ER	3.5			dB	
Average launch power of OFF transmitter, each lane		Poff			-30	dBm	
Optical Return Loss Tolerance		ORL			15.6	dB	
Transmitter reflectance					-26	dB	

1. The typical wavelengths compliant with 1310nm CWDM wavelength grids.

Optical – Receiver

Parameter		Symbol	Min	Typical	Max	Unit	Remarks
Lane wavelengths		λ	1264.5		1277.5	nm	
			1284.5		1297.5		
			1304.5		1317.5		
			1324.5		1337.5		
Average Receiver Power, each lane (P_{avg})			-9		5.1	dBm	
Receiver Overload (P_{avg})		P_{OL}	5.1			dBm	
Damage Threshold (P_{avg})			6.1			dBm	
Receive power, each lane (OMA outer)		OMA			4.4	dBm	
Receiver Sensitivity each lane (OMA outer)	for TECQ<1.4dB				-6.8	dBm	1
	for 1.4≤TECQ≤3.9dB				-8.2+ TECQ	dBm	1
LOS De-Assert		LOS_D			-10	dBm	
LOS Assert		LOS_A	-16			dBm	
LOS Hysteresis			0.5			dB	

1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E-4.

Electrical – Transmitter

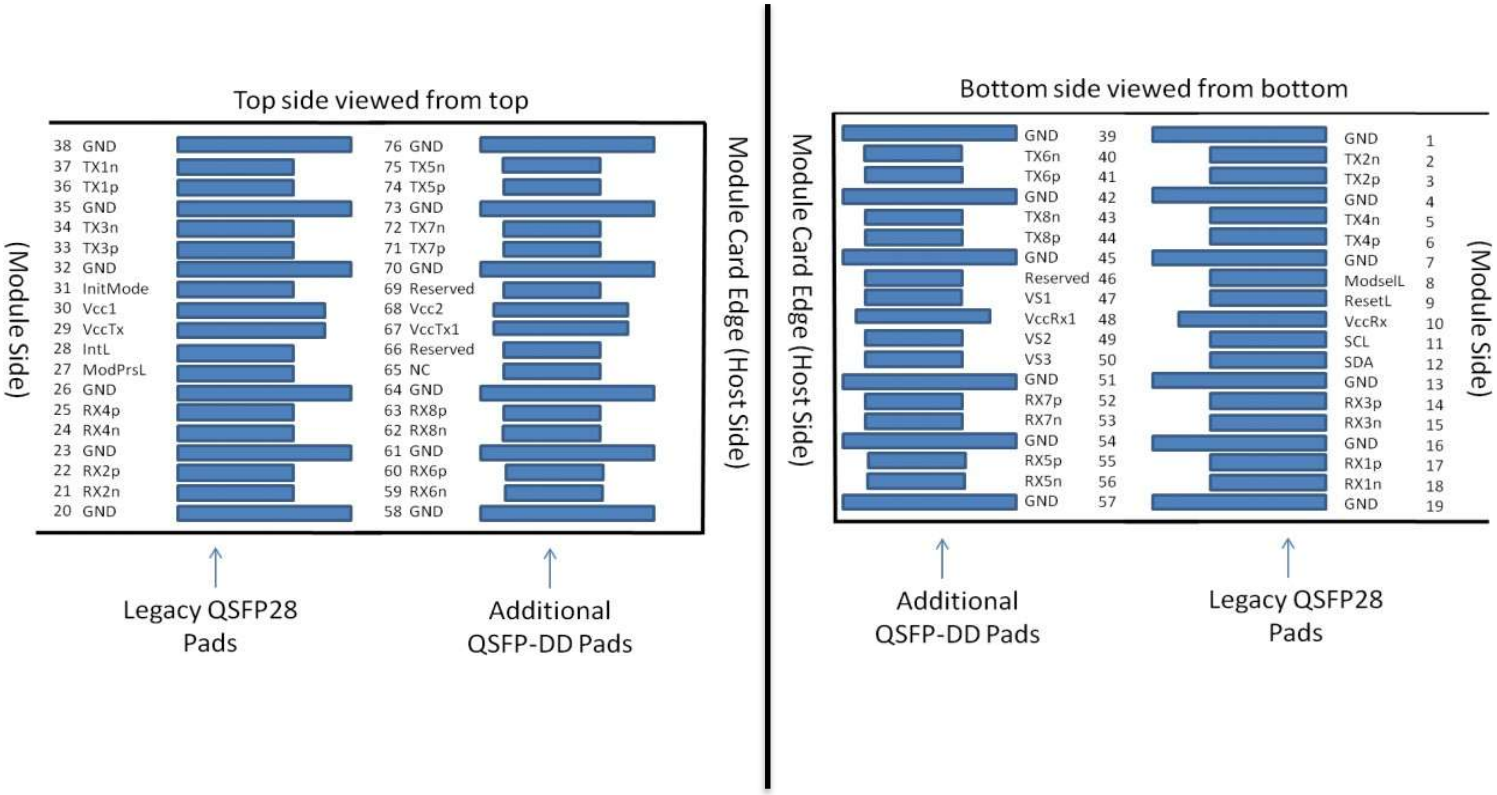
Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Module Supply Current	Icc			2.55	A	
Power Dissipation	P_D			8.0	W	
Input Differential Impedance	Z_{IN}		100		Ω	
Differential Data Input Swing	$V_{IN, P-P}$	180		900	mV_{P-P}	

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Output Differential Impedance	Z_O		100		Ω	
Differential Data Output Swing	$V_{OUT, P-P}$	300		850	mV_{P-P}	1
Transition Time (20% to 80%)	T_r,T_f	9.5			ps	

1. Internally AC coupled but requires an external 100Ω differential load termination.

Electrical Connector Layout



Electrical Pin Definition

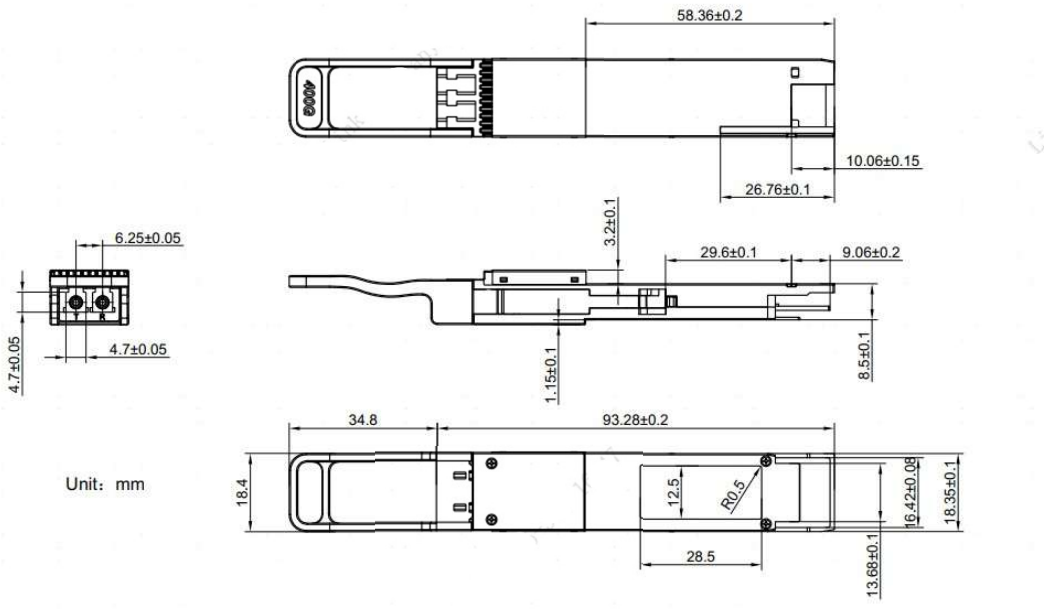
PIN #	Symbol	Description	Remarks
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	

15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1

62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10kohms and less than 100pF.

Mechanical Dimension



Revision History

Date	Rev	Description
12/21/2021	1.0	Release version
02/12/2025	2.0	New branding guidelines

For more information

Vitex LLC 32 Mercer St
Hackensack, NJ 07601

201-296-0145
info@vitextech.com
www.vitextech.com