800G OSFP 2DR4 Optical Transceiver

PN: VO-8CDR4CP-AA

Product Overview

Vitex VO-8CDR4CP-AA are designed for use up to 8x100G PAM4 data rates over 500m single mode fiber. They are designed according to 800 Gigabit Hot-pluggable OSFP Multi-Sourcing Agreement (MSA) standards.

Features

- 8x100G PAM4/8x50G PAM4 data rates
- Hot-pluggable OSFP form factor
- Power dissipation: <16W
- Electrical interface compliant with 100Gbps per lane defined by IEEE 802.3ck
- I2C Management interface compliant to CMIS Rev5.0
- Compliant with IEEE Std 802.3 400GBASE-DR4
- Internal CDR on both Transmitter and Receiver channels
- OSFP MSA package with Dual MPO-12 connectors
- Cooled 1310 EML Laser
- Up to 500m on 9/125um SMF
- Single +3.3V power supply
- Class 1 laser safety certified
- Operating case temperature range: 0oC to 70oC
- RoHS6 Compliant

Applications

- High speed storage area networks
- 2x400G-DR4 applications
- 2x200G-DR4 applications

Ordering Information

Part Number	Description
VD-8CDR4CP-AA	800G QSFP-DD 2DR4, 500m SMF, 1310nm, Dual MPO12, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	5		95	%	
Supply Voltage	V_{CC}	-0.5		3.6	V	
Operating Case Temperature	T_C	0	40	70	°C	
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate			106.25		Gb/s	
			53.125		Gb/s	

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Average Launch Power, Each Lane	P_o(100G)	-2.9	-	4	dBm	1
	P_o(50G)	-5.1		3	dBm	1
Outer Optical Modulation Amplitude, each lane	P_1 (100G)	-0.8	-	4.2	dBm	1
	P_1(50G)	-3		2.8	dBm	1
Extinction Ratio	EX	3.5	-	-	dB	2,3
Lane wavelengths	λ	1304.5	-	1317.5	nm	4
Side-mode suppression ratio	SMSR	30	-	-	dB	5
Transmitter and dispersion penalty eye closure for 100Gbps PAM4, each lane	TDECQ1			3.4		2
Transmitter and dispersion penalty eye closure for 50Gbps PAM4, each lane	TDECQ2			3.2		3
Launch power in OMAouter minus TDECQ for 100Gbps PAM4, each lane	OMA-TDECQ	-2.2				2
Launch power in OMAouter minus TDECQ for 50Gbps PAM4, each lane	OMA-TDECQ	-4.4				3
Average Launch Power of OFF transmitter	Poff				-15	
Optical Return Loss Tolerance	ORLT				21.4	
Transmitter Reflectance					-26	

1. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
2. 106.25Gbps PAM4.
3. 53.125Gbps PAM4.
4. 13nm width.
5. Modulated.

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Lane wavelengths	λ	1304.5		1317.5	nm	
100G Receiver Sensitivity (OMA)	RxSENS1			-3.9	dBm	1
50G Receiver Sensitivity (OMA)	RxSENS2			-6.1	dBm	2
Receiver Overload, each lane (Pavg)	POL	4			dBm	
Damage Threshold, each lane		5			dBm	
Receive power, each lane (OMAouter)	OMA			4.2	dBm	
Receiver Reflectance				-26	dB	
LOS De-Assert	LOSD			-10	dBm	
LOS Assert	LOSA	-16			dBm	
LOS Hysteresis		0.5			dB	

1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E^{-4}.
2. Measured with PRBS31Q test pattern, 26.5625GBd, PAM4, BER<2.4E^{-4}.

Electrical – Transmitter

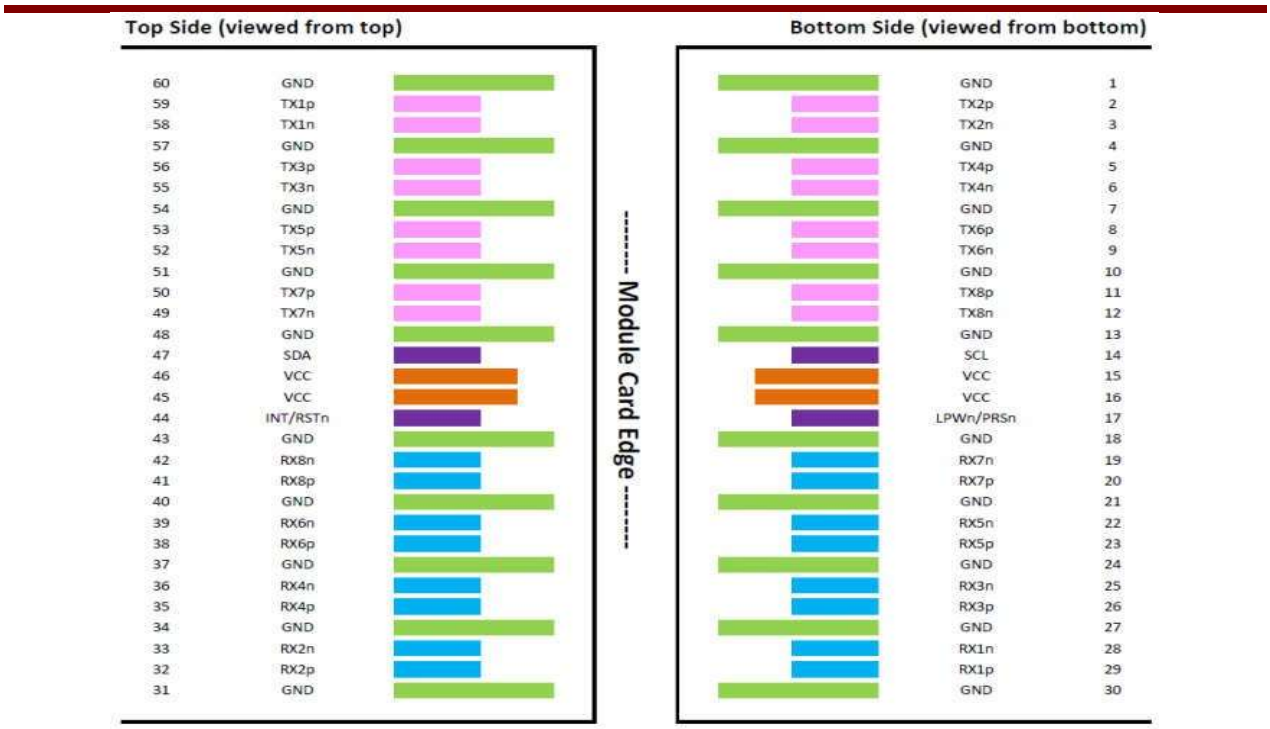
Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Module Supply Current	Icc		4.5	5.1	A	
Power Dissipation	PD		14.85	16	W	
Input Differential Impedance	ZIN	90	100	110	Ω	
Differential Data Input Swing	VIN, P-P			900	mVP-P	
DC Common-Mode Input Voltage		-350		2850	mV	

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Output Differential Impedance	Z_O	90	100	110	Ω	
Differential Data Output Swing	$V_{OUT, P-P}$			900	mV_{P-P}	1

1. Internally AC coupled but requires an external 100Ω differential load termination.

Electrical Connector Layout



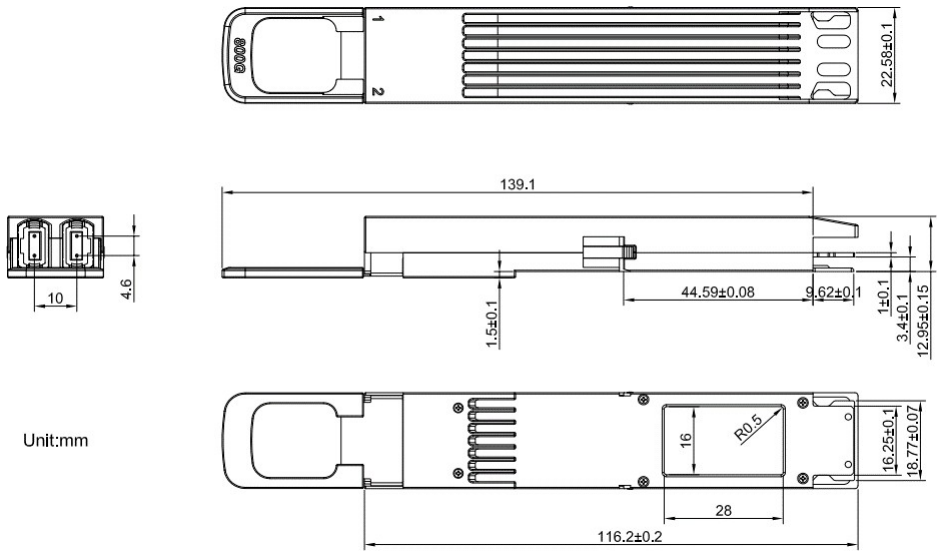
Electrical Pin Definition

PIN #	Symbol	Description	Logic	Direction	Plug Sequence	Remarks
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	2
18	GND	Ground			1	

19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	2
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	1
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

1. Open-Drain with pull-up resistor on host.
2. See pin description of OSFP MSA for required circuit.

Mechanical Dimension



Revision History

Date	Rev	Description
04/09/2023	1.0	Release version
02/13/2025	2.0	New branding guidelines

For more information

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