800G OSFP 2DR4++/LR4 Optical Transceiver
PN: VO-8CLR4CP-AA

Product Overview

Vitex VO-8CLR4CP-AA are designed to be used at up to 8x100G PAM4 data rates over 10km single mode fiber. These transceiver modules are compliant with 800 Gigabit Hot-pluggable OSFP Multi-Sourcing Agreement (MSA) standards.

Features

- 8x100G PAM4 data rate
- Hot-pluggable OSFP form factor
- 7nm DSP for low power dissipation: <16W
- Cooled 1310 EML Laser
- Electrical interface compliant with 100Gbps per lane defined by IEEE 802.3ck
- I2C Management interface compliant to CMIS Rev5.0
- Compliant with IEEE Std 802.3cu 100GBASE-LR1
- Internal CDR on both Transmitter and Receiver channels
- OSFP MSA package with Dual MPO-12 connectors
- Up to 10km on 9/125um SMF
- Single +3.3V power supply
- Class 1 laser safety certified
- Operating case temperature range: 0 °C to 70 °C
- RoHS6 Compliant

Applications

- High speed storage area networks
- 2x400G-PLR4 applications

Ordering Information

Part Number	Description
VO-8CLR4CP-AA	800G OSFP 2DR4++/LR4, 10km SMF, 1310nm, Dual MPO12, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	5		95	%	
Supply Voltage (Maximum)	V_{CC}	-0.5		3.6	V	
Operating Case Temperature	T_C	0	40	70	°C	
Supply Voltage (Recommended)	V_{CC}	3.135	3.3	3.465	V	
Data Rate			106.25		GBps	

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Lane wavelengths	λ	1304.5		1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane	P	-1.9		4.8	dBm	
Transmitter and dispersion penalty eye closure for PAM4, each lane	TDECQ			3.4	dB	
Outer Optical Modulation Amplitude, each lane for TDECQ<1,4dB	OMAouter	1.1		5	dBm	
For 1.4 dB < TDECQ < 3.4 dB		-0.3+ TDECQ		5	dBm	
Extinction Ratio	ER	3.5			dB	
Average launch power of OFF transmitter	Poff			-15	dBm	
Optical Return Loss Tolerance	ORLT			15.6	dB	
Transmitter reflectance				-26	dB	

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Lane wavelengths	λ	1304.5		1317.5	nm	
Receiver Sensitivity each lane (OMAouter), for TECQ<1.4dB				-6.1	dBm	1
For 1.4 < TECQ < 3.4dB				-7.5+TECQ	dBm	1
Receiver Overload, each lane (P_{avg})	P_{OL}	4.8			dBm	
Damage Threshold, each lane		5.8			dBm	
Receive power, each lane (OMAouter)	OMA			5	dBm	
Receiver Reflectance				-26	dB	
LOS De-Assert	LOSD			-10	dBm	
LOS Assert	LOSA	-16			dBm	
LOS Hysteresis		0.5			dB	

1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E-4.

Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Module Supply Current	Icc			5.1	A	
Power Dissipation	PD			16	W	
Input Differential Impedance	ZIN	90	100	110	Ω	
Differential Data Input Swing	VIN, P-P			900	mVP-P	

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Output Differential Impedance	ZO	90	100	110	Ω	
Differential Data Output Swing	VOUT, P-P			900	mVP-P	1

1. Internally AC coupled but requires an external 100Ω differential load termination.

Electrical Connector Layout

Electrical Pin Definition

PIN #	Symbol	Description	Logic	Direction	Plug Sequence	Remarks
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	2
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	

43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	2
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	1
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

1. Open-Drain with pull-up resistor on host.
2. See pin description of OSFP MSA for required circuit.

Mechanical Dimension

Unit:mm
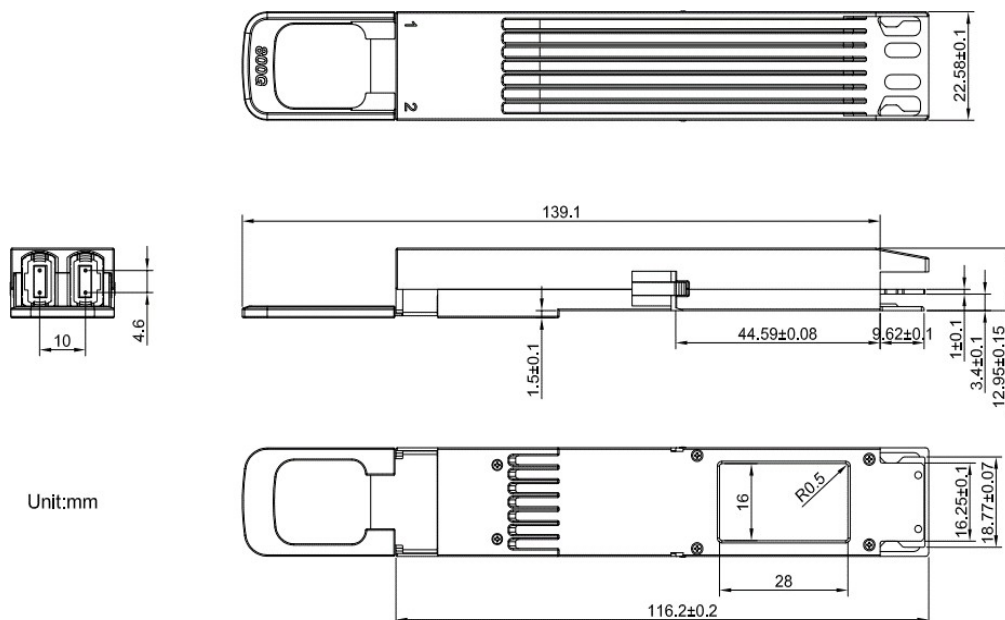
Revision History

Date	Rev	Description
04/09/2023	1.0	Release version
02/13/2025	2.0	New branding guidelines

For more information

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