

800G OSFP SR8 Optical Transceiver PN: VO-8CSR8CP-ANA

Product Overview

Vitex VO-8CSR8CP-ANA, 800G SR8 OSFP-RHS transceiver, is a hot-pluggable OSFP 800G SR8 multimode transceiver featuring an integrated 850nm VCSEL array and PD array, designed to comply with IEEE 802.3ck and IEEE 802.3db standards, adhering to OSFP RHS specifications, and equipped with dual MPO-12 or MPO16 connectors.

Features

- Hot-pluggable OSFP 800G SR8 multimode transceiver
- Integrated 850nm VCSEL array and PD array
- IEEE 802.3ck, IEEE 802.3db
- Compliant with OSFP RHS
- Dual MPO-12 or MPO16 connector
- Compliant with CMIS Rev 4.0 and beyond
- Maximum power consumption 15W
- Single 3.3V power supply
- Case operating temperature: 0°C to 70°C
- Compliant to RoHS
- Class 1 Laser Safety

Ordering Information

Part Number	Description
VO-8CSR8CP-ANA	OSFP 800G SR8 Flat Top RHS, 30m MMF, 850nm, Dual MOP12, C-temp

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General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	
Storage Temperature	TS	-40		85	°C	
Supply Voltage (Maximum)	Vcc	-0.5		3.6	V	
Relative Humidity (non-condensing)	RH	5		95	%	
Control Input Voltage	VI	-0.3		VCC+0.5	V	
Operating Case Temperature	TOPR	0		70	°C	
Power Supply Voltage (Recommended)	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP			6800	mA	
Sustained peak current at hot plug	ICC_SP			5670	mA	
Maximum Power Dissipation	PD			15	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signaling Rate per Lane	SRL		53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate		-100		1000	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)				66	mV	
Rx Differential Data Output Load			100		Ohm	

Optical - Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Wavelength	λС	844	850	863	nm	
RMS spectral width	Δλrms			0.6	nm	
Average Launch Power, each lane	AOPL	-1.0		3.0	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane	ТОМА	-2.1		3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			4.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF			-30	dBm	
Extinction Ratio, each lane	ER	2.5	3.5		dB	
RIN]4OMA	RIN			-148	dB/Hz	
Optical Return Loss Tolerance	ORL			14	dB	
Transmitter Reflectance	TR			-26	dB	



Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Wavelength	λС	842	850	863	nm	
Damage Threshold, average optical power, each lane	AOPD	5			dBm	
Average Receive Power, each lane	AOPR	-6.3		4.0	dBm	
Receive Power (OMA _{outer}), each lane	OMAR			3.5	dBm	
Receiver Reflectance	RR			-20	dB	
Receiver Sensitivity (OMAouter), each lane	SOMA			-4.6	dBm	
Stressed Receiver Sensitivity (OMAouter), each lane	SRS			-2.0	dBm	
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	
OMAouter of each aggressor lane	OMAouter		3.5		dBm	

Electrical – Transmitter

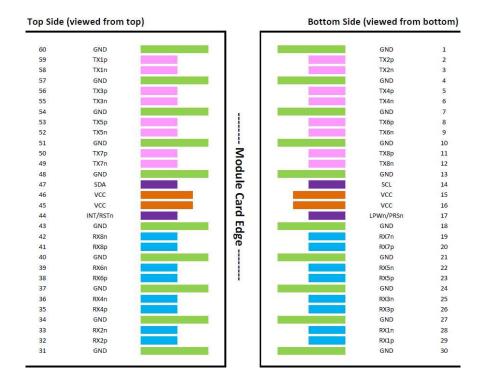
Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Differential pk-pk input Voltage tolerance (TPla)		750			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common-mode voltage		-350		2850	mV	

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
AC common-mode output Voltage (RMS)				25	mV	
Differential output Voltage (Long mode)				845	mV	
Differential output Voltage (Short mode)				600	mV	
Near-end Eye height, differential		70			mV	
Far-end Eye height, differential		30			mV	
Far end pre-cursor ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	



Electrical Connector Layout



Electrical Pin Definition

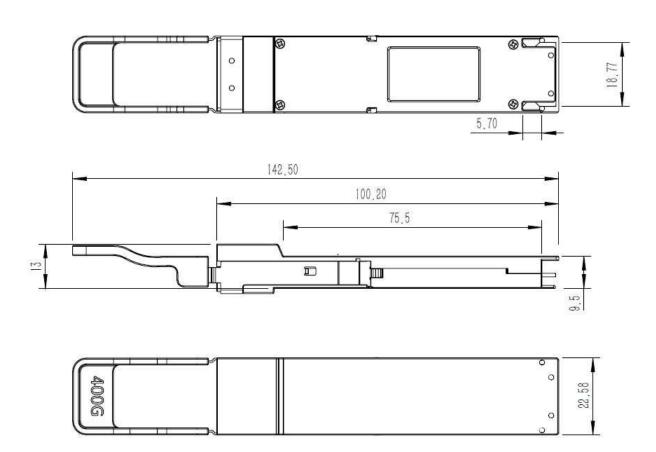
PIN#	Logic	Symbol	Description	Direction	Plug Seq.	Notes
1		GND	Ground		1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	Input from Host	3	
3	CML-I	TX2n	Transmitter Data Inverted	Input from Host	3	
4		GND	Ground		1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	Input from Host	3	
6	CML-I	TX4n	Transmitter Data Inverted	Input from Host	3	
7		GND	Ground		1	
8	CML-I	ТХ6р	Transmitter Data Non-Inverted	Input from Host	3	Not used
9	CML-I	TX6n	Transmitter Data Inverted	Input from Host	3	Not used
10		GND	Ground		1	
11	CML-I	тх8р	Transmitter Data Non-Inverted	Input from Host	3	Not used
12	CML-I	TX8n	Transmitter Data Inverted	Input from Host	3	Not used
13		GND	Ground		1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	Bi-directional	3	
15		VCC	+3.3V Power	Power from Host	2	
16		VCC	+3.3V Power	Power from Host	2	

			pecification	Di diventional	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	3	
18		GND	Ground		1	
19	CML-O	RX7n	Receiver Data Inverted	Output to Host	3	Not use
20	CML-O	RX7p	Receiver Data Non-Inverted	Output to Host	3	Not use
21		GND	Ground		1	
22	CML-O	RX5n	Receiver Data Inverted	Output to Host	3	Not use
23	CML-O	RX5p	Receiver Data Non-Inverted	Output to Host	3	Not use
24		GND	Ground		1	
25	CML-O	RX3n	Receiver Data Inverted	Output to Host	3	
26	CML-O	RX3p	Receiver Data Non-Inverted	Output to Host	3	
27		GND	Ground		1	
28	CML-O	RX1n	Receiver Data Inverted	Output to Host	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	Output to Host	3	
30		GND	Ground		1	
31		GND	Ground		1	
32	CML-O	RX2p	Receiver Data Non-Inverted	Output to Host	3	
33	CML-O	RX2n	Receiver Data Inverted	Output to Host	3	
34		GND	Ground		1	
35	CML-O	RX4p	Receiver Data Non-Inverted	Output to Host	3	
36	CML-O	RX4n	Receiver Data Inverted	Output to Host	3	
37		GND	Ground	-	1	
38	CML-O	RX6p	Receiver Data Non-Inverted	Output to Host	3	Not us
39	CML-O	RX6n	Receiver Data Inverted	Output to Host	3	Not us
40		GND	Ground	·	1	
41	CML-O	RX8p	Receiver Data Non-Inverted	Output to Host	3	Not us
42	CML-O	RX8n	Receiver Data Inverted	Output to Host	3	Not us
43		GND	Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	3	
45		VCC	+3.3V Power	Power from Host	2	
46		VCC	+3.3V Power	Power from Host	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	Bi-directional	3	
48	21011100 1/0	GND	Ground		1	
49	CML-I	TX7n	Transmitter Data Inverted	Input from Host	3	Not us
50	CML-I	TX711	Transmitter Data Non-Inverted	Input from Host	3	Not us
51	CIVIL I	GND	Ground		1	1.00 40
	CML			Input from Uset		Not · · ·
52	CML-I	TX5n	Transmitter Data Inverted	Input from Host Input from Host	3	Not us
53	CML-I	TX5p	Transmitter Data Non-Inverted	input non nost	1	NOL US
54	<u> </u>	GND	Ground			
55	CML-I	TX3n	Transmitter Data Inverted	Input from Host	3	
56	CML-I	TX3p	Transmitter Data Non-Inverted	Input from Host	3	

VO-8CSR8CP-ANA Product Specification

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57		GND	Ground		1				
58	CML-I	TXln	Transmitter Data Inverted	Input from Host	3				
59	CML-I	ТХІр	Transmitter Data Non-Inverted	Input from Host	3				
60		GND	Ground		1				

Mechanical Dimension



Revision History

Date	Rev	Description
07/26/2020	1.0	Release version
02/18/2025	2.0	New branding guidelines

For more information

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