

100G QSFP28 PSM4 Optical Transceiver

PN: VQ-1CFR4CP-AA

Product Overview

Vitex VQ-1CFR4CP-AA is designed for up to 2km reach service with four-lane 25.78125G data rate. It is compliant with QSFP MSA, SFF-8436, SFF-8636 and PSM4 MSA standards. Digital diagnostic functions are available via the I2C interface.

Features

- MPO-12 optical interface
- Maximum link length up to 2km
- Up to 25.78125 Gbps data links per lane
- +3.3 V power supply
- QSFP MSA compliant package
- Hot Pluggable
- High performance signal mode DML transmitter
- High sensitivity PIN/TIA optical receiver
- Single Mode operation
- $BER < 5E-5 @ -10.5dBm$ (OMA)
- Built-in CDR
- Case Operating temperature: 0 to 70°C
- Data and Control Interfaces
- Tx & Rx Data CML/AC Coupled
- ModSelL LVTTTL / ResetL LVTTTL / ModPrsL LVTTTL / LPMode LVTTTL
- 2-wire I2C communication bus
- RoHS 6 compliance

Applications

- 100G BASE Ethernet
- Infiniband EDR interconnects
- Enterprise networking

Ordering Information

Part Number	Description
VQ-1CFR4CP-AA	100G QSFP28 PSM4, 2km SMF, 1310nm, MPO12, C-temp

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	
Storage Temperature	T_{stg}	-40		+95	°C	
Case Operating Temperature (Commercial)	T_O	0		+70	°C	
Relative Humidity - Storage	RH_s	0		95	%	
Relative Humidity - Operating	RH_o	0		85	%	
Supply Voltage (Maximum)	V_{cc}	-0.3		3.6	V	
Case Operating Temperature	T_{case}	0		+70	°C	
DC Supply Voltage	V_{cc}	3.135		3.465	V	
Module Supply Current	I_{IN}			1060	mA	

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	
Signal Rate (Each Lane)		25.78125±100ppm			Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_{tol}			8.5	dBm	
Average Launch Power (Each Lane)	P_{avg}	-6.5		2.5	dBm	
Optical Modulation Amplitude (Each Lane)	OMA			2.5	dBm	1
Transmitter and dispersion Penalty (Each Lane)	TDP			2.2	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				1
Average launch power of OFF Transmitter (Each Lane)				-30	dBm	
Extinction Ratio	ER	3.5			dB	
Spectral Width (20dB)				1	nm	
Transmitter Reflectance				-12	dB	
Optical return loss tolerance				20	dB	

1. Hit ratio of 5e-5, per IEEE.

Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	
Signal Rate (Each Lane)		25.78125±100ppm			Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Damage threshold (Each Lane)	THd			3.0	dBm	1
Sensitivity OMA Each Lane	Sen			-10.5	dBm	2
Receiver reflectance				-26	dBm	2
LOS Assert	LOSA	-24				
LOS Deassert	LOSD			-11.6		
LOS Hysteresis	LOSH	0.5		6		

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly with this input power.
2. Measured with conformance test signal at receiver input for BER = 5e-5 BER.

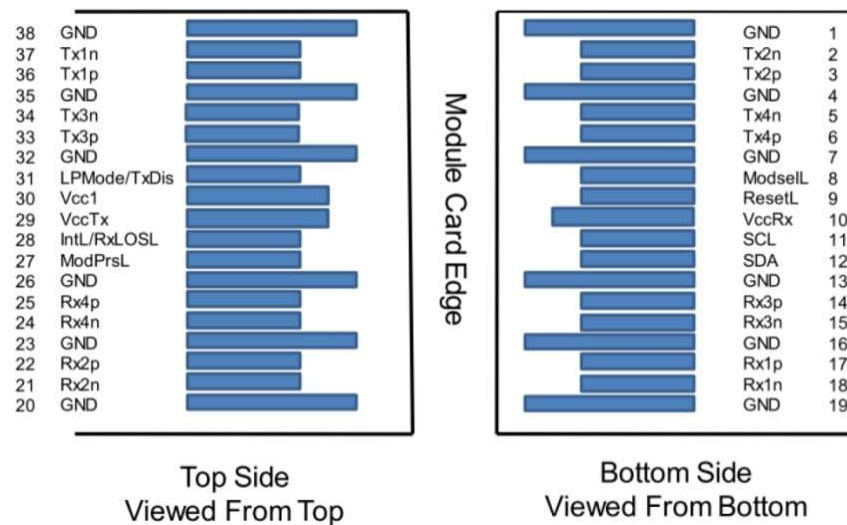
Electrical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit
Differential Data input Swing	V _{IN}	180		900	mV
Tx Differential Input Impedence	Z _{in}	90	100	110	Ω
Tx Differential Output Impedence	Z _{out}	45	50	55	Ω
ResetL Disable Voltage	V _r	2.0		V _{CC} +0.3	V
ResetL Enable Voltage	V _{rEN}	0		0.8	V
ModSelL Disable Voltage	V _m	2.0		V _{CC} +0.3	V
ModSelL Enable Voltage	V _{mEN}	0		0.8	V

Electrical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit
Differential Data Output Swing	V _{OUT}	180		900	mV
Rx Differential Output Impedence	Z _{OUT}	90	100	110	Ω
IntL Assert Voltage	V _{Int}	V _{CC} -0.5		V _{CC} +0.3	V
IntL De-assert Voltage	V _{DInt}	0		+0.4	V

Electrical Connector Layout



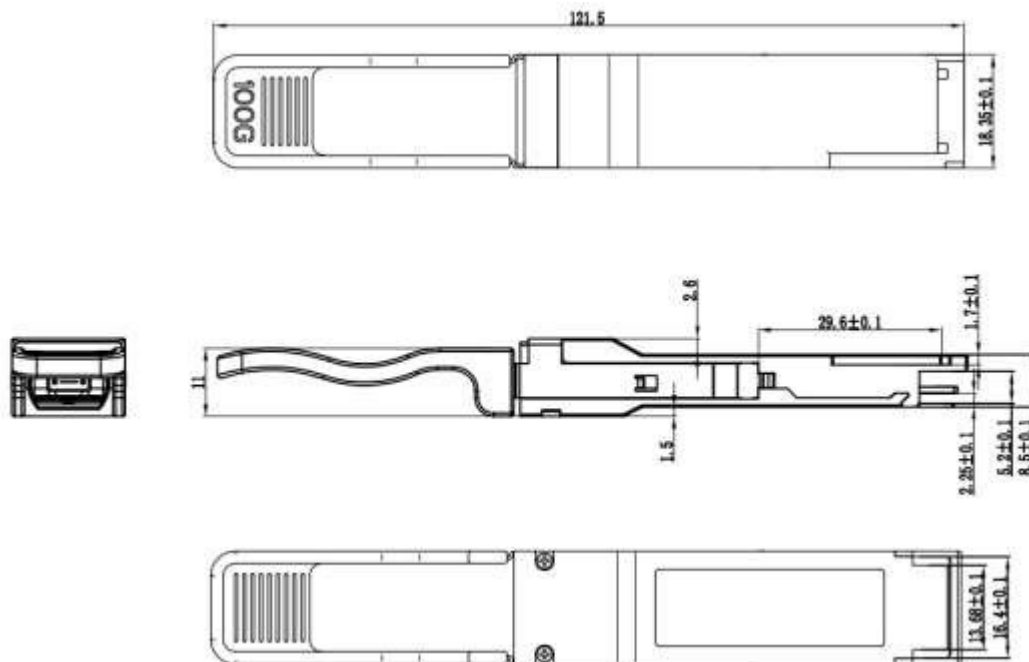
Electrical Pin Definition

PIN #	Logic	Symbol	Description	Remarks
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1

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24	CML-O	Rx2n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTLL-O	ModPrsL	Module Present	
28	LVTLL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		VccI	+3.3V Power Supply	2
31	LVTLL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Mechanical Dimensions



Revision History

Date	Rev	Description
09/20/2023	1.0	Release version
02/17/2025	2.0	New branding guidelines

For more information

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