
200G QSFP SR4 Optical Transceiver

PN: VQ-2CSR4CP-ANA / VQ-2CSR2CP-ANA

Product Overview

Vitex VQ-2CSR4CP-ANA & VQ-2CSR2CP-ANA are transceivers in a hot-pluggable form factor, compliant with 200G-SR4 & SR2 optical specifications. They feature 4x53.125Gb/s electrical interfaces, integrate an 850nm VCSEL array and PD array with DSP, and supports up to 60m reach on MMF OM3 and 100m on OM4, utilizing a single MPO12 connector

Features

- Hot-pluggable QSFP112 SR4/SR2 multimode transceiver
- Compliant with QSFP112 MSA
- Compliant with CMIS Rev 4.0 and above revision
- Compliant with IEEE P802.3db
- 4-channels of 100G-PAM4 electrical and optical modulation
- Maximum power consumption 8.5W with 4 channels and 6.5W with 2 channels
- Up to 60m reach on OM3 and 100m reach on OM4
- Single MPO-12 APC receptacles
- Case operating temperature 0°C to 70°C

Ordering Information

Part Number	Description
VQ-2CSR4CP-ANA	200G QSFP112 SR4, 100m MMF, 850nm, MPO12, C-temp
VQ-2CSR2CP-ANA	200G QSFP112 SR2, 100m MMF, 850nm, MPO12, C-temp

Note: This datasheet contains product information for both Vitex PN VQ-2CSR4CP-ANA and VQ-2CSR2CP-ANA.

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Storage Temperature	T _S	-40		85	°C	
Power Supply Voltage (Maximum)	V _{CC}	-0.4		3.6	V	
Relative Humidity (non-condensing)	RH	5		85	%	
Operating Case Temperature	TOPR	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Supply Voltage	ICC	-	-	3190	mA	
Maximum Power Dissipation(400G)	PD	-	-	8.5	W	
Maximum Power Dissipation(200G)	PD	-	-	6.5	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance (OM3)	D1	-	-	60	m	
Operating Distance (OM4)	D2	-	-	100	m	

Optical – Transmitter

Parameter	Symbol	Min	Typical	Max	Unit	Remarks
Average launch power, each lane	AOPL	-4.6		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each lane	TOMA	-2.6		3.5	dBm	2
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.4	dB	
Average Launch Power of OFF Transmitter, each lane	ToFF			-30	dBm	
Extinction ratio, each lane	ER	2.5	-	-	dB	
RIN _{OMA}	RIN	-	-	-132	dB/Hz	
Transmitter Reflectance	TR	-	-	-26	dB	3
Optical return loss tolerance		-	-	-12	dB	

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if max (TECQ, TDECQ) < 1.8dB, OMA_{outer} (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

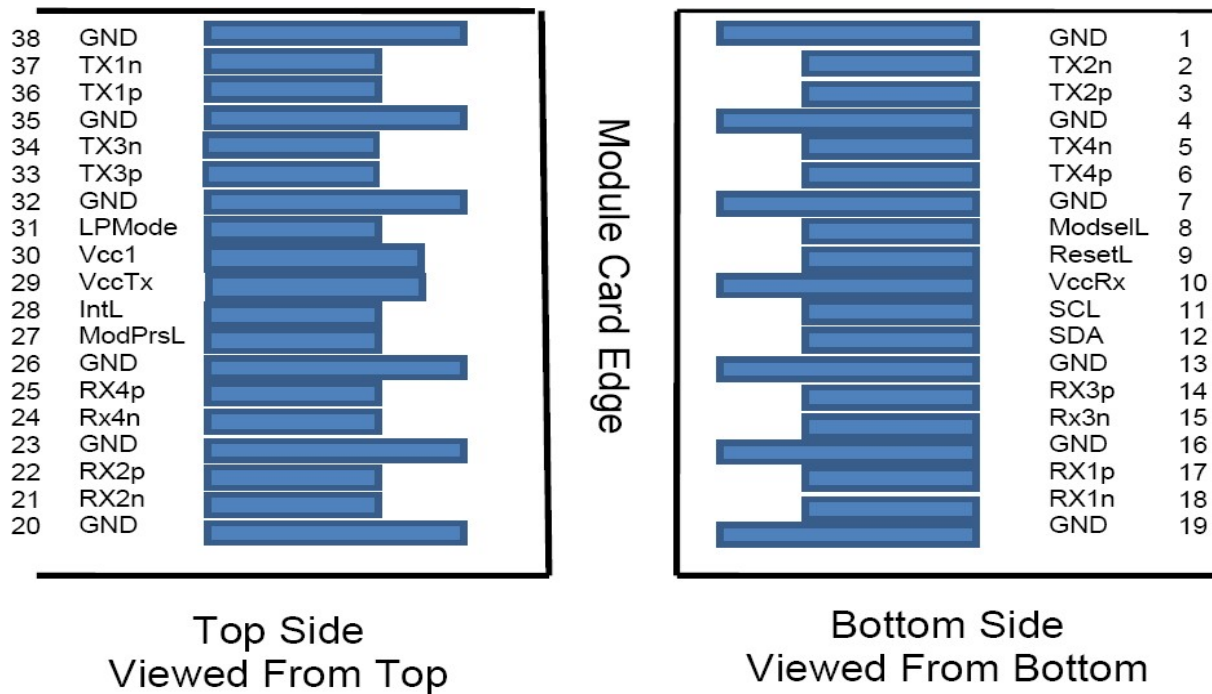
Optical – Receiver

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λ _C	842	-	863	nm	
Average receive power, each lane	AOP _R	-6.4	-	4	dBm	1
Receive power, each lane (OMA _{outer})	OMA _R	-	-	3.5	dBm	
Receiver reflectance	R _R		-	-26	dB	
Receiver sensitivity (OMA _{outer}), each lane	SOMA		-	-4.4	dBm	2
Stressed receiver sensitivity (OMA _{outer}), each lane	SRS		-	-1.8	dBm	3
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4	SECQ		4.4		dB	

OMA _{outer} of each aggressor lane	OMA _{outer}	3.5	dBm
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1. Minimum power is informative. AOP above the minimum does not ensure compliance
2. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴

Electrical Connector Layout



Electrical Pin Definition

PIN #	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	

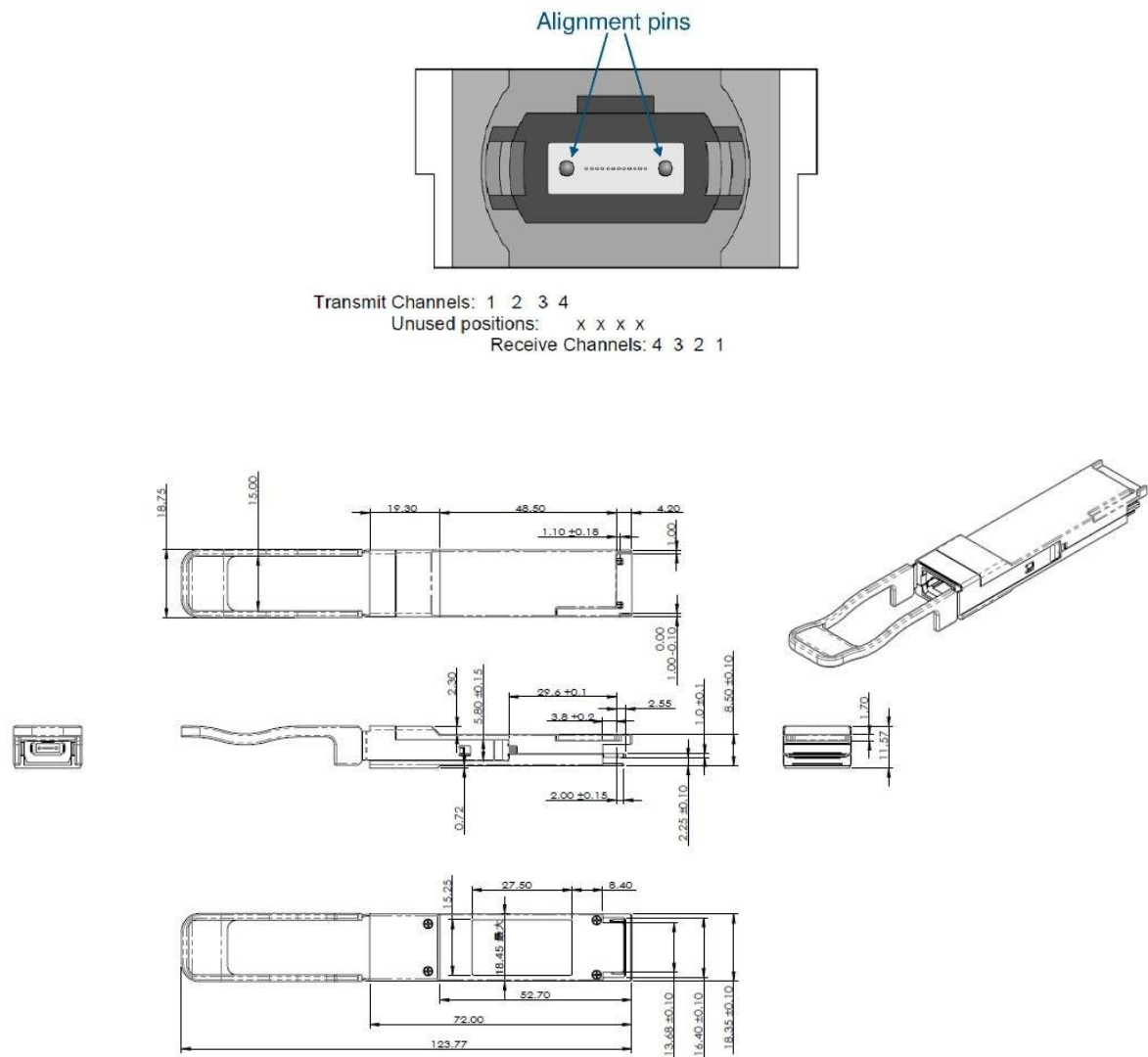
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13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		VccI	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1. GND is the symbol for signal and supply (power) common for the QSP56 module. All are common within the QSP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, VccI and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Recommended host board power supply filtering is shown in below Figures. Vcc Rx VccI and Vcc Tx may be internally connected within the QSP56 Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Mechanical Dimension



Revision History

Date	Rev	Description
07/26/2020	1.0	Release version
02/18/2025	2.0	New branding guidelines

For more information

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